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A STUDY OF CHARGED PARTICLES/RADIATION DAMAGE TO VLSI DEVICE MATERIALS

FINAL REPORT

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ABSTRACT

Future spacecraft systems such as the manned space station will be subjected to low-dose long term radiation particles, such as electrons, protons and alpha particles. Most electronic systems are affected by such particles. When electronic devices are subjected to radiation, their electrical properties may change to the extent that the devices may become nonfunctional for a short period of time or may even suffer permanent damage. As advances are made in VLSI processes and the feature size of electronic devices continues to decrease towards the submicron level, the devices will become more susceptible to single event upsets. There is therefore a great need to understand device physics and failure mechanisms affected by radiation and to design circuits that would be less susceptible to radiation. This work addresses these concerns.

Using 2MeV electron radiation and bias temperature aging, it was found that MOS capacitors that have been pre-positively biased have lower flatband voltage shift and lesser increase in density of surface state charge than those that were not pre-positively biased. In addition, it was shown that there is continued recovery of flatband voltage and density of state charge in irradiated capacitors during both room temperature anneal and 137^{o} anneal.

When nMOS transistors were subjected to 1 MeV proton radiation, charge pumping and current versus voltage measurements indicated that transconductance degradation, threshold voltage

shifts and changes in interface states density may be the primary cause of nMOS transistor failure after radiation. In addition, it was found that secondary radiation effects are significant to cause device failure.

Furthermore, simulation studies using SPICE were performed on CMOS SRAM cells of various transistor sizes. It is shown that transistor sizing affects the noise margins of CMOS SRAM cells, and that as the beta ratio of the transistors of the CMOS SRAM cell decreases, the effective noise margin of the SRAM cell increases. Some suggestions were made in connection with the design of CMOS SRAMS that are hardened against single event upsets.

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NOMENCLATURE

A	Gate Area
C_{hf}	High Frequency Capacitance
C_{it}	Interface Trap Capacitance
C_{lf}	Low Frequency Capacitance
C_{ox}	Oxide Capacitance
Dit	Interface States Density
E_g	Band Gap
E_f	Fermi Level
E_c	Conduction Band Energy
E_v	Valence Band Energy
E_i	Intrinsic Fermi Level
f	Frequency
I_{cp}	Charge Pumping Current
K	Boltzmann's Constant
m	Segregation Coefficient
Na	Number of Acceptor Concentrations
Nit	Interface States Charge
q	Electronic Charge
Qit	Interface Trapped Charge
Qot	Oxide Trapped Charge
Qss	Surface States Charge
Q_f	Fixed Charge
Si	Silicon
SiO_2	Silicon Dioxide
t_f	Fall time

t_r	Rise Time
Tp	Peak Period
Tb	Base Period
Qs	Surface Potential
V_{FB}	Flat Band Voltage
Vg	Gate Voltage
V_{gp}	Peak Level of Gate Waveform
V_{gb}	Base Level of Gate Waveform
V_{TH}	Threshold Voltage
Gm	Transconductance
E	Energy
Vs	Power Supply Voltage
Vnit	Threshold Voltage Shift due to Interface States
Vnot	Threshold Voltage Shift due to Oxide Trapped Charge

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SUMMARY AND CONCLUSIONS

This work deals with the study of device physics and failure mechanism affected by electron and proton radiation. In addition, the design of circuits that are less susceptible to single event upsets is considered. This work is divided into three main parts. The first is concerned with the determination of the effect of electron radiation on MOS capacitors using capacitance versus voltage measurements. The second part investigates the hole transport phenomena, the density of interface traps and their distribution in energy space when MOS transistor was subjected to proton radiation. The third part deals with the design of CMOS SRAM cells that are hardened against single event upsets.

Chapter 1 discusses space environment and sources of radiation in space. This includes ionizing radiation, proton radiation in MOS devices, general discussion on single event upset (SEU), flatband voltage shifts and transconductance degradation in VLSI devices. Also given in Chapter 1 is a literature review of MOS device response to radiation.

The characterization of the effect of radiation on MOSFET devices using capacitance-voltage (C-V) measurements is provided in Chapter 2. The application of capacitance-voltage method for determining mobile ion contamination, trapped charge, flatband voltage shift and surface state charge is discussed. Using 2MeV electron radiation and bias temperature aging method, it was found that MOS capacitance structures that have been pre-

positively biased have lower flatband voltage shift and lesser increase in density of surface state charge than those devices that were not pre-positively biased. In contrast to an investigator's claim that there is no significant change in density of surface state charge during anneal, this work showed that there is continued recovery of flatband voltage and density of surface state charge in irradiated capacitors during both room temperature anneal and 137^{o} C anneal. A mechanism has been proposed to explain this observation.

To obtain a better understanding of hole transport phenomena, the density of interface traps and their distribution in the upper and lower half of the silicon band gaps of the MOSFET, the charge pumping technique was employed. It is shown that transconductance degradation, threshold voltage shifts, changes in interface states density that do occur after 1 MeV proton radiation in MOS devices may be the primary cause of the device failure after radiation. In addition, it is shown that even if the 1MeV proton is shielded by the package, secondary radiation effects are sufficient to cause device failure. Furthermore, in contrast with the normal positive charge associated with donor states in the lower half of the band gap, it was seen that there is a build-up of proton radiation induced negative charge at at $Si-SiO_2$ interface when the n-channel devices were based to inversion.

The effect of transistor sizing on hardening CMOS Static Random access memory (SRAM) against single event upsets (SEU) was investigated in Chapter four. Simulation studies using SPICE was performed on CMOS SRAM cells of various transistor sizes. The

effective noise margins of the circuits were calculated. It was found that as the geometrical beta ratio of the transistors decreases, the effective noise margin of the SRAM cells increases. The results seen to indicate that CMOS SRAM is more hardened against SEUs as the beta ratio of the transistors is decreased. It was also confirmed that CMOS SRAM with feedback resistors are more hardened against SEUs than CMOS SRAM cell without feedback resistors.

CHAPTER I

INTRODUCTION AND LITERATURE REVIEW

1.1 MOTIVATION

The great emphasis NASA is placing on the development of manned space station necessitates the understanding of the device and system radiation resistance to low level, long time duration radiation environment. Cosmic rays, high energy protons and electrons in the inner and outer Van Allen Belts affect electronic components in spacecrafts. As a result of radiation, there can be a transient change in the operation of a electronic system or a permanent damage to some of the electronic parts. There is threfore a great need to understand the device physics and failure mechanisms of irradiated devices and also to design electronic systems that would be unaffected by radiation.

1.2 THE SPACE ENVIRONMENT

In space, three prominent environments are encountered. The first and most important is the Van Allen radiation belt, which consists of energetic electrons and protons trapped by the earth's magnetic field. The proportions of each of these and their respective energy spectrum vary considerably with location and time. Next is the solar radiation which consists of plasma of electrons and protons spraying radially out from the sun. The last is cosmic radiation, which is a very low flux of very high-energy particles from the cosmos. Of these, the electrons and protons of the Van Allen belt are present in sufficient quanti-

ties to be significant in considering damage to MOS device structures. Many of the charged particles (electrons and protons) are deflected by the earth's magnetic field and others are absorbed. The damage induced in the MOS devices subjected to a radiation environment is of sufficient magnitude that degradation of the electrical characteristics of these devices must be considered in space exploration. The effects of radiation on MOS devices are classified as surface or bulk effects depending upon the damage mechanism involved. Bulk effects arise from the production of electron-hole pairs in the semiconductor crystal by ionizing radiation, and from the production of defects in the crystal lattice by high energy particles. Theoretically, surface effects arise from the ionization of the encapsulating gas and the interaction of this ionized gas with the surface of the semiconductor material. In the case of the electron-hole pair creation in the oxide and the inherent hole trapping; interaction with interface states becomes an important factor.

1.2.1 IONIZING RADIATION

Ionizing radiation may be defined as radiation capable of producing free electron and positive ions or holes. It includes gamma rays,, X-rays, cosmic rays, and high energy electrons and protons. The effects of these particles range from temporary digital upsets (soft errors, and single event upsets) to permanent digital upsets (latch-ups), to total dose dependent parameter shifts and finally to chemical alterations.

Cosmic rays are charged particles (ions) that move at high velocities and come toward the earth from all directions in

space. Many of the lower speed cosmic-ray particles come from the sun. These are called solar cosmic rays. They are probably blown out of the sun by violent explosions. Much slower protons and electrons--the "solar wind"--are streaming continuously out of the sun in large numbers. The higher energy cosmic rays coming from all directions probably originate in our Milky Way Galaxy and are called galactic cosmic rays. They pass right through spacecraft at a rate of 2 particles/(cm^2) hr. All of these particles are deflected by the earth's magnetic field. The slow, light ones are deflected more than the fast, heavy galactic cosmic-ray particles.

The direction of travel of a charged particle is changed by the magnetic field. The cosmic ray in the upper right of Fig. 1.1 is thus deflected downward. Such deflections of cosmic rays produce the "latitude effect" (Cosmic rays are more intense at north and south high latitudes than near the equator).

Defections of slower moving ions--the protons and electrons--in the solar wind are larger, and the earth's magnetic field has "captured" many of them in the Van Allen belt (named after physicist James Van Allen of the University of Iowa, who discovered it from measurements on the Explorer 1 satellite in 1958).

The cutaway view of Fig. 1.1 shows the doughnut shaped regions where protons and electrons are oscillating north and south along the magnetic line of force (dashed lines) [1]. These charged particles spiral around the lines of force at speeds of several kilometers per second and are deflected back where the

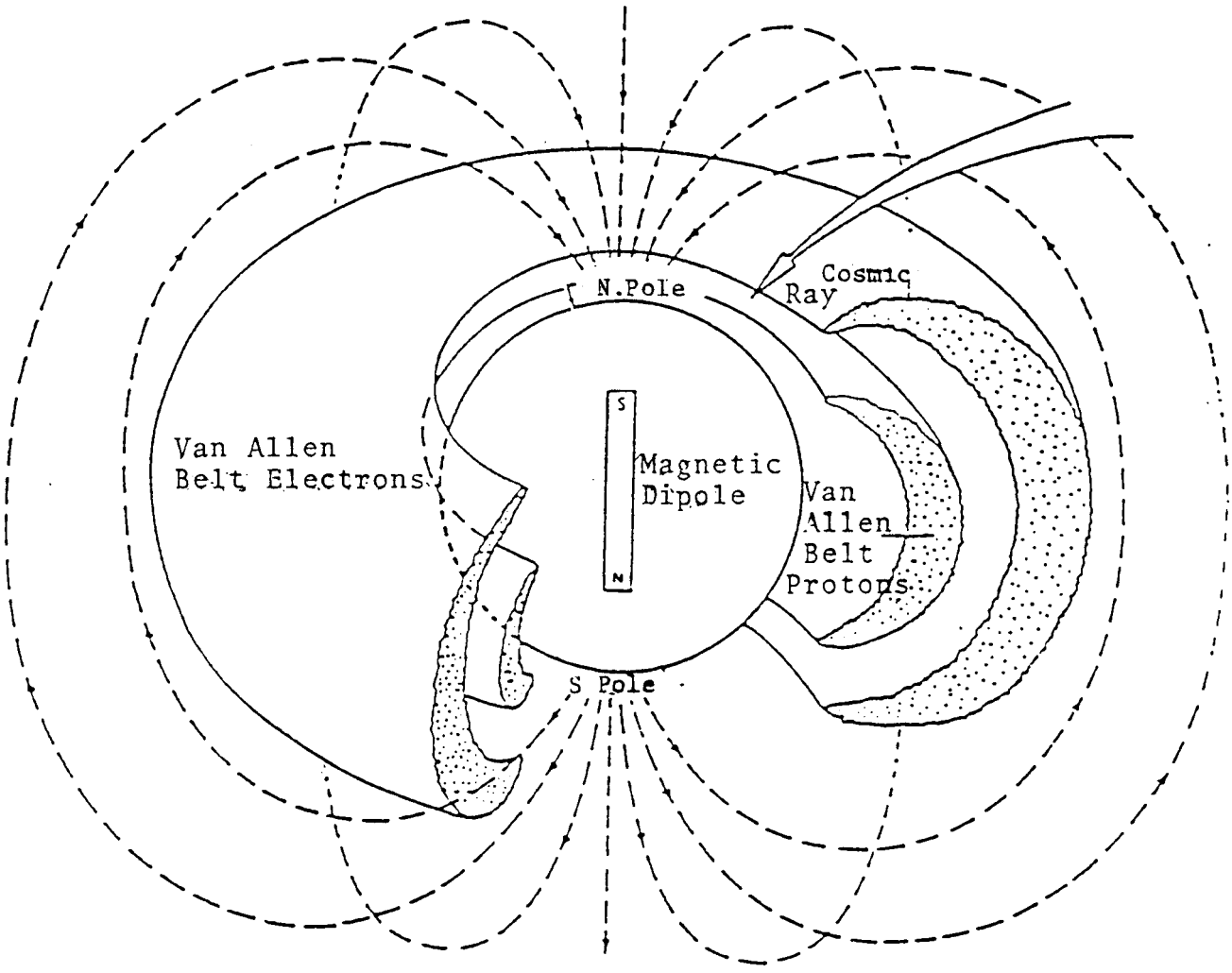


Figure 1.1 Radiation Effects in Space
(From Page and Page [1])

lines of force get close near the magnetic poles. There are no sharp boundaries to the regions where protons and electrons are oscillating. The peak intensity of protons occurs at about 3000km latitude where the protons have energies from 1 to 10 MeV. Because of the intensity of this "radiation" in the Van Allen belt, this region is by far the most hazardous to sensitive instrumentation in spacecraft. Significant secondary radiation caused by interaction of these high energy particles with spacecraft structures or electronic encapsulations may enhance the damage.

The outer regions of the earth's magnetic field are affected by the solar wind, and the "magnetosphere"--the region of the upper atmosphere that is dominated by the earth's magnetic field--has a shock front" facing into the wind (more or less toward the sun) and a "tail" stretching downwind. More important for spacecraft, the earth's magnetic field has a "dent" over the Atlantic Ocean just east of Brazil that causes the Van Allen belt to bulge downward toward the earth's surface in a region called the South Atlantic Anomaly. This irregularity in the magnetic field produces a region of very intense radiation in the lower part of the Van Allen belt (about 1000 times more intense than in nearby space). NASA scientists have learned that some instruments on spacecraft give erroneous reading while they are in the South Atlantic Anomaly.

1.2.2 SPACE STATION CONSIDERATIONS

The space station is scheduled to be launched from Kennedy Space Center at an inclination of 28.5 degrees. Its estimated

distance from the earth is 500km or 270 nautical miles At this inclination, the spacecraft will be angled away from the polar regions where the protective shield of the earth's magnetosphere and the Van Allen Belts would be absent. The space shuttle will most likely be in orbit below the inner Van Allen Belt and the majority of particles will be 1 to 10MeV protons. In the interior of the spacecraft with 2 grams per square inch shielding, the expected dose rate is 75 milligrams per day. The average dosage for multiple passes through the South Atlantic Anomaly with electronic components mounted on the exterior of the spacecraft can be as high as three rads per day.

1.3 PROTON RADIATION IN MOS DEVICES

An understanding of proton radiation damage effects on MOS devcie is very important in considering long term space duration experiments. Protons in space have been shown to produce alpha particles that are responsible for inducing upsets and soft uspset errors. When these particles (protons) pass through an MOS device, its rate of energy loss dE/dx depends on energy as 1/E. As particle reaches the end of its range, its displacement cross-section increases accordingly, resulting in a highly non-uniform defect along the particle's track. Day et al [2], have shown that the range of 250 KeV and 1.5 MeV protons in silicon is about 20 and 30 microns, respectively. As a result, proton damage is very complex, particularly at low energy levels in terms of its effect on transistor terminal behavior.

Exposing MOS devices to high-energy proton radiation can

lead to trapping of holes in the oxide. The radiation ionized the insulator by generating hole-electron pairs. The electrons pass through the oxide-gate interface, while the holes are captured by traps. This effect is complicated when a positive gate voltage is applied during irradiation. Even after the radiation source is removed, a layer of positive charge remains at the Si - SiO_2 interface. This causes a shift in the flat band voltage as well as the threshold voltage. The threshold voltage's negative shift is reduced considerably with increasing radiation dose for an n-channel device, possibly due to acceptor states filling up [3].

Radiation generally can also generate new interface traps and create electron traps near the interface. Four types of charge associated with a thermally grown Si SiO_2 interface are shown in Fig. 1.2.

Although protons (produced indirectly through free carriers generated by in-coming radiation) may be mobile in SiO_2, they do not discharge at electrodes and therefore are not the major cause of mobile positive oxide charge resulting from exposure to ionizing radiation. Because of its rapid transport in SiO_2 and its abundance in the environment, sodium is the most important mobile ion in SiO_2. Interaction between protons and sodium in SiO_2 may have strong influence on the migration of mobile ions.

Chew [4] in his doctoral dissertation, discussed models for interface states generation. One of his models is the introduction of both holes and electrons into the SiO_2 under fields greater than 6-7 MegV/cm. This is the Fowler-Nordheim tunnelling. The mechanism is shown in Fig. 1.3 in which an

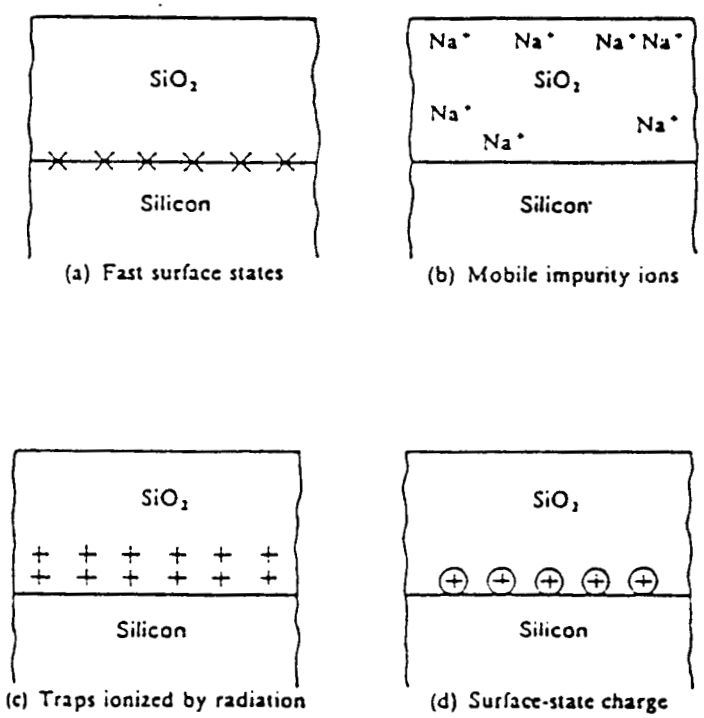


Figure 1.2 Types of Charge Associated with Si--SiO_2 interface (From A.S. Grove [32])

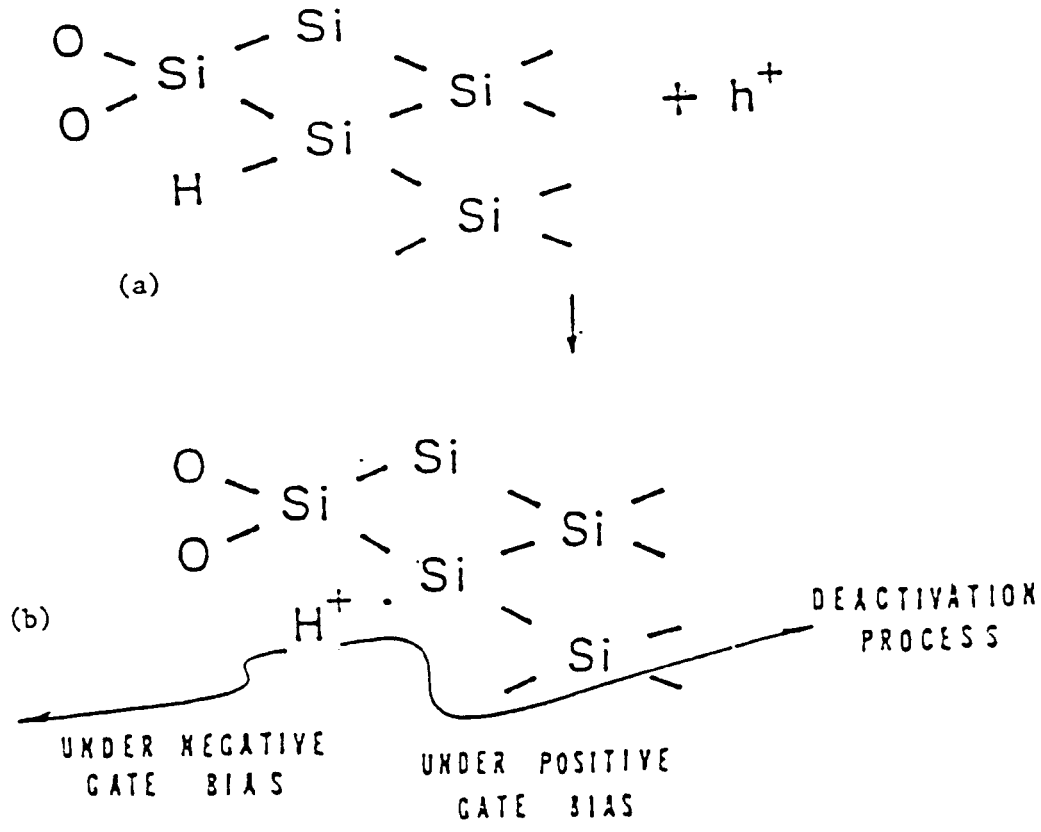


Figure 1.3 Schematic Representation of Interface States Generation Under Fowler-Nordheim Injection

(a) Si-H bond broken by an injected hole and a proton released

(b) Released proton swept by the positive gate bias toward silicon substrate to cause an acceptor deactivation process, or move into oxide under negative gate bias

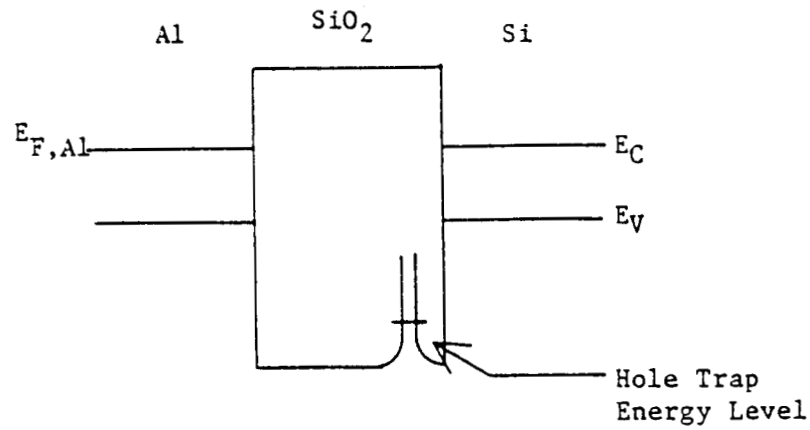
(From H. Chew [4])

injected hole breaks a Si - H bond, thus relasing a proton and creating a dangling bond. The releasing proton is swept toward acceptor deactivation process or move into oxide under negative gate bias.

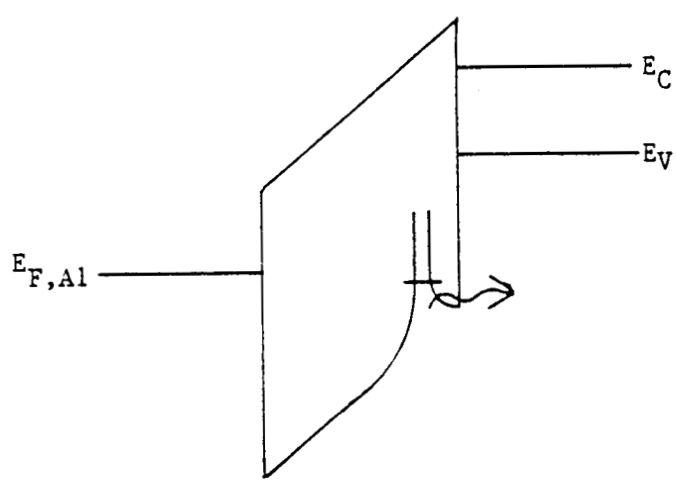
Another mechanism of hydrogen instability which does not require the high fields necessary with Fowler-Nordheim tunnelling is photo injection of electron. A 450^{o}C post metallization hydrogen anneal has proven effective in tying up the dangling bonds and reducing Q_{ss} from in-process radiation. Premetalization hydrogen incorporated in the gate oxide, depending on species may actually induce more traps if the device is exposed to further radiation.

Trombetta [5] presented a hole trap as a potential well extending into the oxide forbidden gap from the valence band and located near the Si - SiO_2 interface as shown in Fig 1.4. Upon application of bias, the height of the energy barrier between the hole and the substrate is decreased and the probability of tunnelling is increased.

Although several models exist for interfacial traps, experimer support the idea that interfacial traps exist because of unsatisfied or dangling bonds at the surface of the semiconductor. The effect of proton radiation on an n-channel MOS device will be discussed in Chapter 3 as a result of various tests that were conducted.



(a)



(b)

Figure 1.4 Hole Trap Potential Well
(a) under zero bias , (b) under positive gate bias
(From L. Trombetta [5])

1.4 RADIATION DEFECTS IN MOSFET DEVICE

The influence of high level proton radiation on semiconductor materials produces a quasi-stable change in the properties of such materials. This change stems from primary radiation induced defects such as dangling bonds, vacancies, interstitials and disordered regions (DR) whose interaction with various imperfections of the material give rise to a wide range of active centers, rebound effects and resulting threshold voltage shifts, as well as single event upset. It has been shown that the amount of energy lost by a proton impinging on the semiconductor material varies with its energy and the material.

In the MOS device structure, the areas of interest to this work are the silicon, silicon-silicon dioxide interface and the silicon dioxide phases. In a single silicon crystal, defects are dependent on crystal orientation and impurity concentration. Defects in the Si -SiO_2 interface are valence orientation-pair type. The O_3 center creates the electron trapping and the O_1 fects create trapping centers. Dangling silicon bonds are also classified as a defect. The E centers, nonbridging oxygen hole center (NBOHC) and peroxy radicals are defects found in the SiO_2. Pb centers are expected to be trivalent silicon.

1.4.1 DEFECT IN SILICON DIOXIDE

Three fundamental defects that are identified in both normal SiO_2 and -SiO_2 include the E1 center, the non-bridging oxygen hole centers (NBOHC) and the peroxyl radical (PR). The E1 center is an oxygen vacancy with a hole trapped primarily on one of the silicon atoms nearest the vacancy. The unpaired electron

remaining on the other silicon is Electron Paramagnetic Resonance (EPR) active. The NBOHC, as its name implies, is a trapped hole on a singly coordinated O^{-2} ion. The peroxyl radical is a trapped hole on a singly coordinated O molecule ion.

The peroxyl radical exhibits surprising behavior in that, for temperatures below about 400^{o} C, the concentration of this defect grows with annealing temperature and with radiation dose, while in this temperature range the concentrations of NBOHC and E1 centers decrease.

Of all these defects, only E1 and Pb center has been tested theoretically. Recently, theoretical treatment of the peroxyl radical has been presented by Edwards and Fowler [6], and it was found to depend on the results for the NBOHC and E1 centers, since the hole trapping is responsible for creation of the peroxyl radical. The peroxyl radical can be formed in the following ways:

(1) Initial radiation creates oxygen vacancies, free oxygen atoms, and free electrons and holes. Some of these free oxygen atoms and holes are trapped by bridging oxygen atoms to form a peroxyl radical.

(2) The holes are also trapped at oxygen vacancies to form E1 centers. Some of the oxygen atoms combine to form O_2 which enhances the pre-existing concentration of interstitial O_2. The O_2 can combine with centers to form a more stable peroxyl radical.

1.4.2 ELECTRONIC STRUCTURE OF SiO_2 WITH DEFECTS

Because of its relevance to MOS devices and applications, silicon dioxide and its structure have been the subject of numerous theoretical and experimental investigations dealing with intrinsic defects (mainly the E1 center) in both crystalline and non-crystalline forms of the material. Fig. 1.5 summarizes much that is known or inferred about the electronic structure of SiO_2 with defects. The band gap is determined from photoconductivity measurement, whereas the structure and width of the valence band is determined from photoelectronic spectroscopy. It can be reasoned that the energy of a dangling Sp^3 silicon hybrid orbital (ie, the E center) must lie somewhere within the band gap, and that oxygen-associated trapped-hole states must lie near or just above the top of the valence band.

S.A. Lyons et al. [7], proposed that amphoteric Pb centers are type of defects that account for all the interface states due to trapped holes, precausing photo injection or grown oxide. Figure 1.6 shows Pb center on silicon (100) and silicon dioxide interface.

The excited state of the E1 center (E^{1} *) lies below the conduction band edge since the excitation into the familiar E' center does not produce photocurrent. Various details of the data are best explained by assuming the formation of E centers, most of which decay by the rehealing of broken Si-O bonds.

The formation of E' centers in SiO_2 layers of irradiated MOS devices has been shown to be a substantial source of the space charge build-up responsible for device degradation under

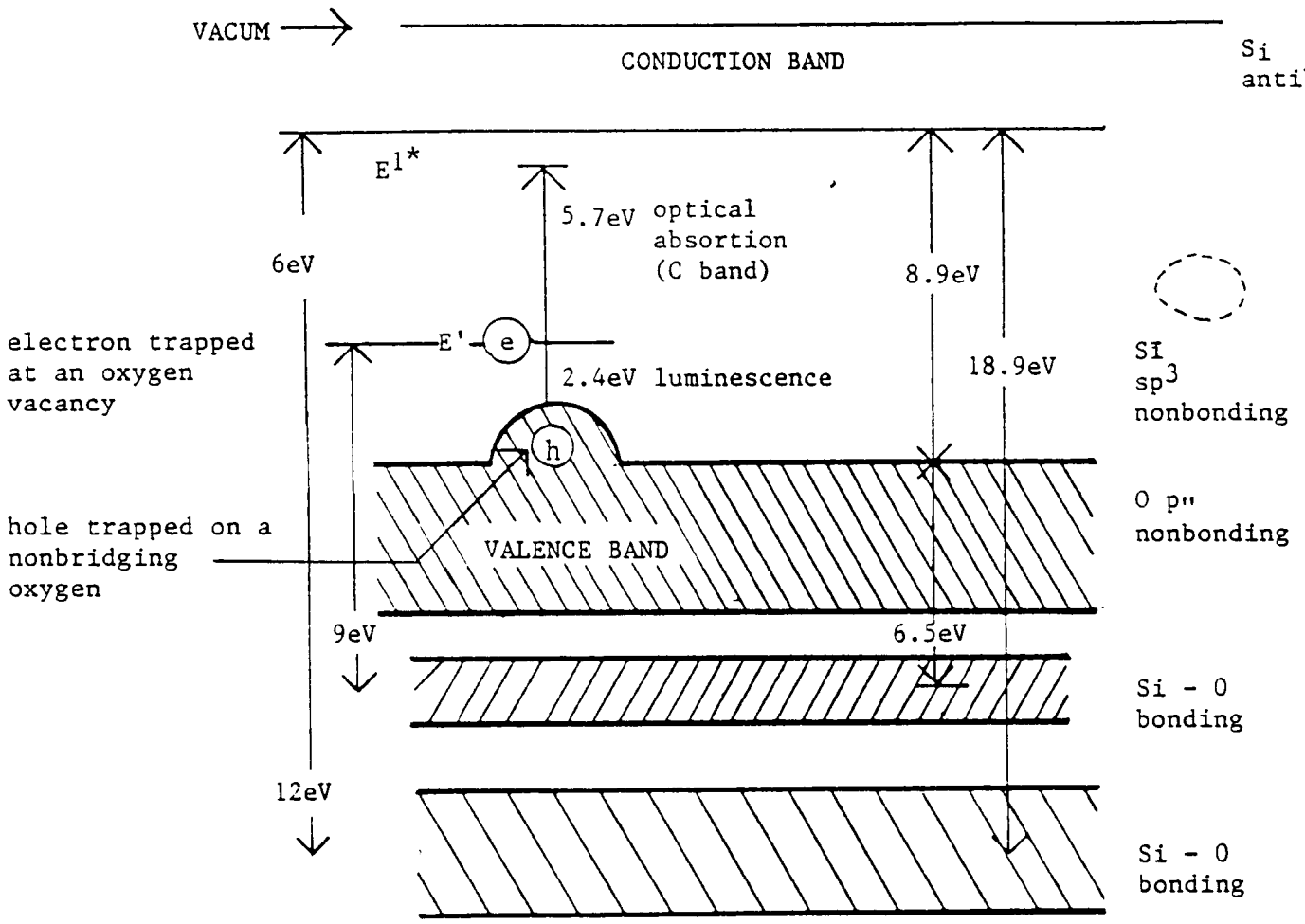


Figure 1.5 Electronic Structure of Silicon Dioxide with Defects

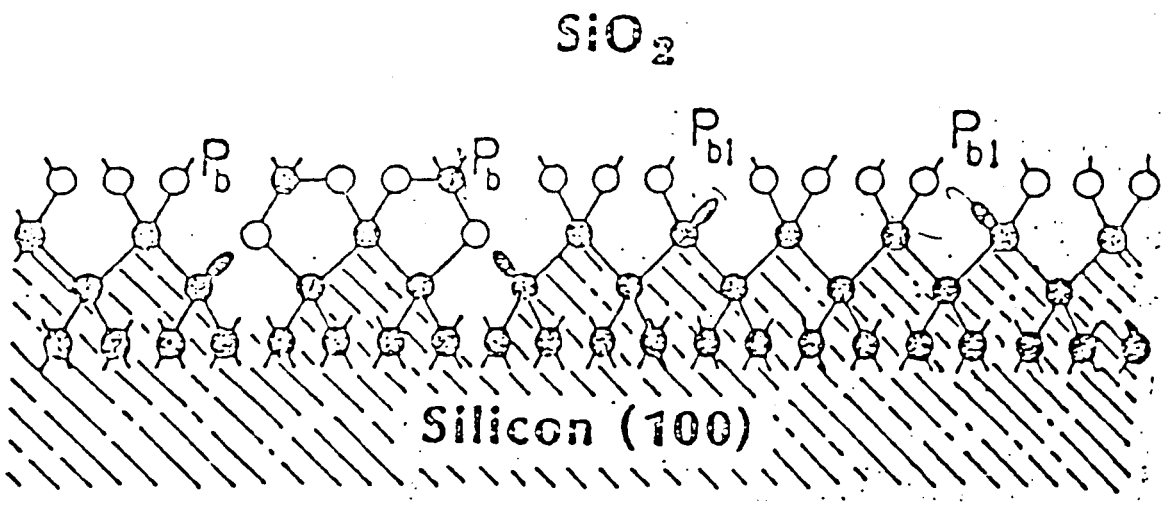


Figure 1.6 Pb Center on Silicon (100) and Silicon Dioxide Interface
(From S.A.Lyon [7])

irradiation.

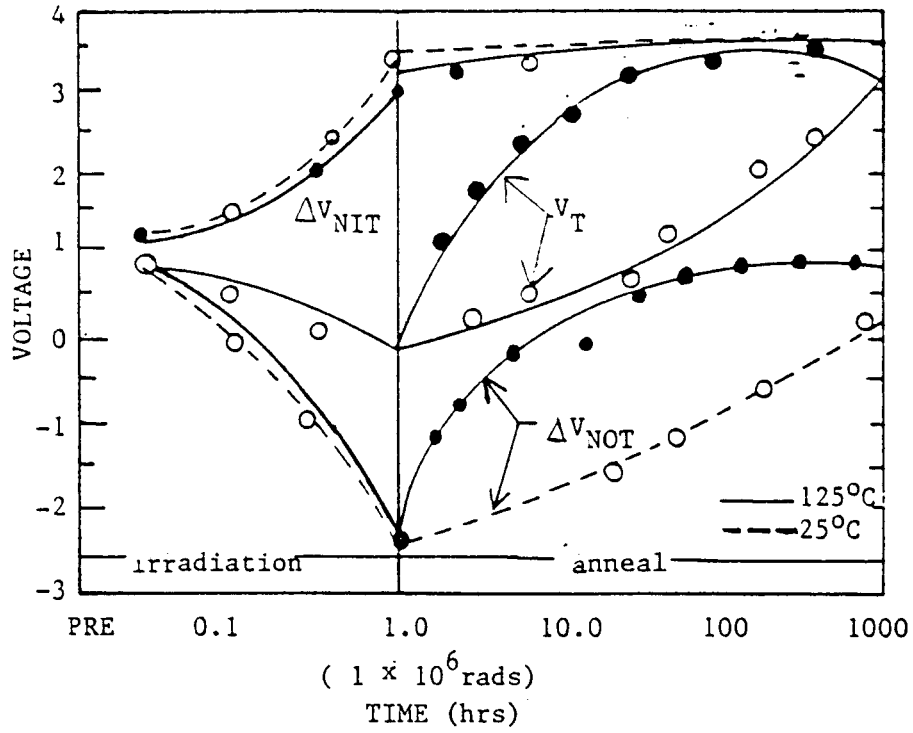
Responding to trends in modern VLSI process technology, several forms of failure mechanisms involving interfacial traps have been proposed to determine VSLI devices parameter variations under the influence of bias temperature aging, irradiation and annealing effects.

1.5 REBOUND PHENOMENON IN MOS DEVICES

It has recently been shown that irradiated MOS devices are subject to a long-term annealing effect known as rebound. This effect occurs during or shortly after irradiation. Rebounds, which can be related to the annealing or creation of oxide trapped charge or interface state charge, cause integrated circuit failures.

Schwank et al [8] have presented the rebound mechanism by separating the threshold voltage shifts into components due to oxide trapped charge, DV_{Not}, and interface trap charge, V_{Nit}. Fig 1.7 shows this separation using an n-channel transistor during irradiation and during bias anneal at room temperature and 125^{o} C. The observed response shows that the threshold voltage decreased to zero volts during radiation, and increased to over 3.5 volts during bias anneal. The net effect shows that during and after irradiation and bias anneal, the threshold voltage shift was due primarily to interface states charge, N_{it}. This means that the positive shift of DV_{nit} is due to negative charging of the upper band gap acceptor state during inversion of the P-type substrate. Fig 1.7(a) and (b) illustrates that oxide trapped charge (positive) anneals out at room temeprature if the

(a)



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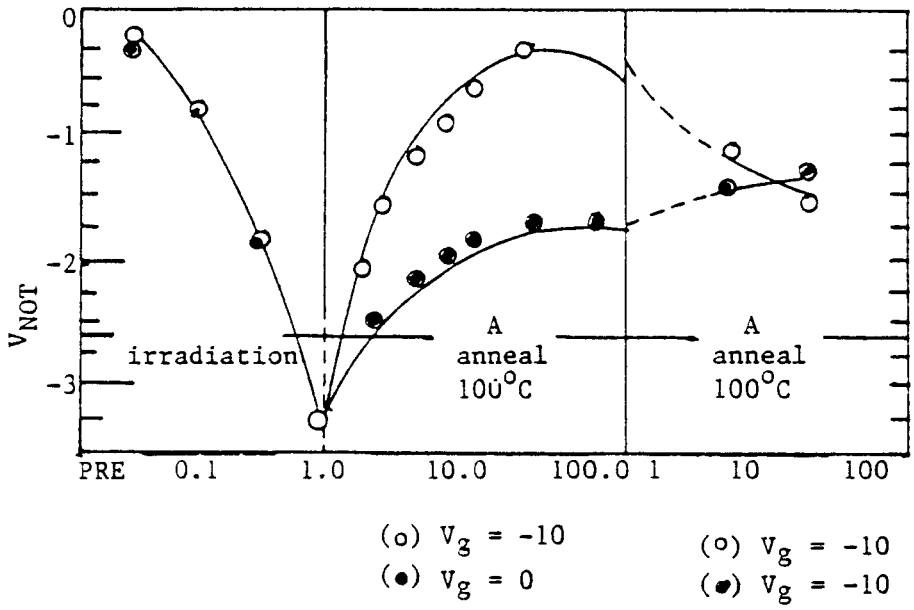


Figure 1.7 Annealing of Transistors
(a) Threshold shift of an N-channel transistor during irradiation and anneal

(b) Anneal of the oxide trapped charge (From Schwank et al. [8])

inversion bias is maintained whereas there is no change in Qit. This rebound may shift more positive than the original irradiation threshold voltage value but if the bias into inversion is removed the negative Qit recovers over several hour time period, negating the rebound effect.

1.6 MOS THRESHOLD VOLTAGE DEGRADATION.

Fig. 1.8 shows threshold voltage as a function of radiation dose for both n-channel and p-channel MOS transistors. The formation of positive oxide charge with increasing dose causes the threshold voltage to decrease for both transistors. This decrease becomes significant above a dose of about 10^4 rads. Above 10^5 rads, the threshold voltage for the n-channel transistor increases, presumably as a result of formation of negative charged interface states. For the p-channel transistor, the formation of positive oxide charge causes the threshold voltage shift to be more negative with increasing dose. This decrease becomes significant above 10^4 rad without the appearance of any compensatng charge. This difference between n-channel and p-channel devices is not well understood. King and Martin [3] proposed that with a +5V irradiation bias the negative shift is eventually overcome by the effect of interface state build-up which becomes important at about 10^5 rad and causes the n-channel threshold to increase. They argued that the n-channel transistor threshold voltage shifts are acceptable as a means of determining a device failure mechanism, but that the p-channel transistor, which has a more significant shift in threshold voltage for the -5V bias condition, can be used to verify both

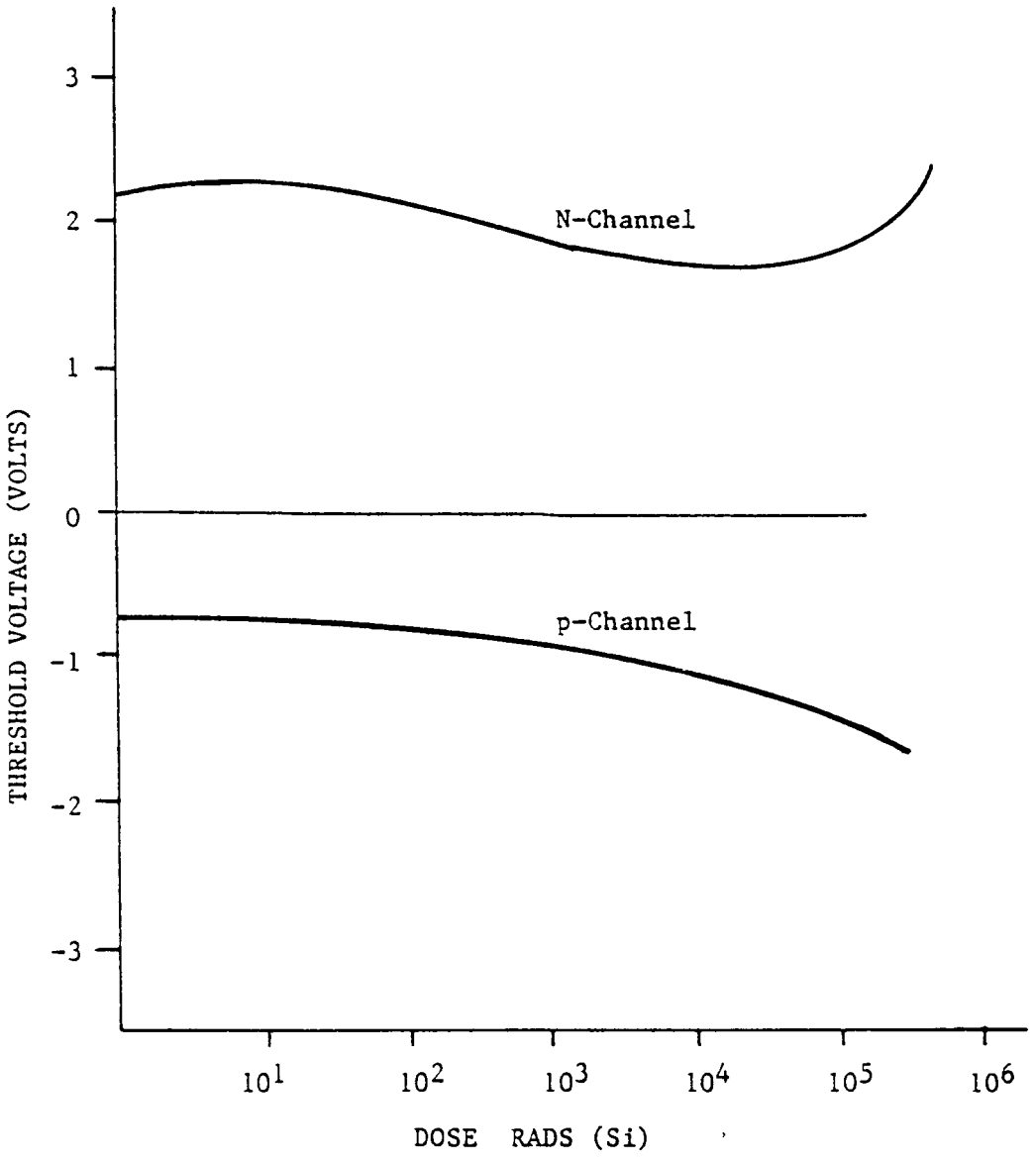


Figure 1.8 Threshold Voltage Versus Total Radiation Dose

the device's failure mechnaism as well as its functional level failure.

We believe that this threshold voltage versus radiation dose result may not be a sure means of testing failure mechanism for an n-channel transistor. Rather, it introduces an adverse effect to the device. Since above 10^5 rads the threshold voltage value exceeds its orignial value, it is doubtful if the device's turn on voltage will be maintained as we expect an alteration in the equilibrium condition at the strong inversion region and a gate dielectric breakdown as a result of possible an electric field increase. The mechanism may be similar to the rebound mechanism studied by Schwank et al. [8] for radiation under inversion bias.

1.7 IMPURITY PROFILE

Radiation environment causes a change in the impurity concentration profile of an MOS device because when silicon and silicon dioxide containing the same impurities are in intimate contact, the impurity concentration adjusts itself such that the chemical potential is equal on both sides of the interface. During thermal oxidation, silicon is continually converted to silicon dioxide and silicon-silicon dioxide advances steadily into the silicon causing a redistribution of the impurities. Redistribution can be determined by the rate of advance of the silicon-oxide interface, the chemical activity coefficient of the impurities and their diffusion coefficient in oxide. The redistribution effect depends on the rate of impurity diffusion and the segregation coefficient "m" defined as ratio of impurity concentration in the silicon to the impurity concentration in the

oxide.

When a device of uniform doping concentation is thermally oxidized, the oxide layer will take up or reject the impurity as it grows, creating a non uniformity in doping concentration. Fig. 1.9 shows that boron tends to be depleted near the surface, while phosphorus tends to "snowplow" and pile up. This effect is most severe, that is, the change in concentration is mos pronounced, for wet oxidation and for oxidation at lower temperatures.

Fogarty and Knotts [9] have proposed that during radiation, boron is redistributed into the oxide, and silicon is replaced by boron (see Fig 1.10). As we know from the segregation coefficient "m" that thermodynamically, there is a driving force for boron to redistribute on glassy oxide side of the interface, if activation energy for this process comes from radiation rather than thermal oxidation, then one might expect boron to interchange with silicon in the glass and not be compensated by oxygen stochiometry as in thermal oxide growth, thus leading to a meta-stable non bridging oxygen. Possibly this non-bridging oxygen acts as a negative fixed charge creating O^- and OH^-. Similarly, the particulate silicon near the interface acts as a positive fixed charge.

There may be an additional mechanism for negative charges near the interface and longer relaxation would be expected than in acceptor interface states of the rebound mechanism. This might fit the relaxation times for rebound effects better than the fast states models proposed by Schwank et al [8].

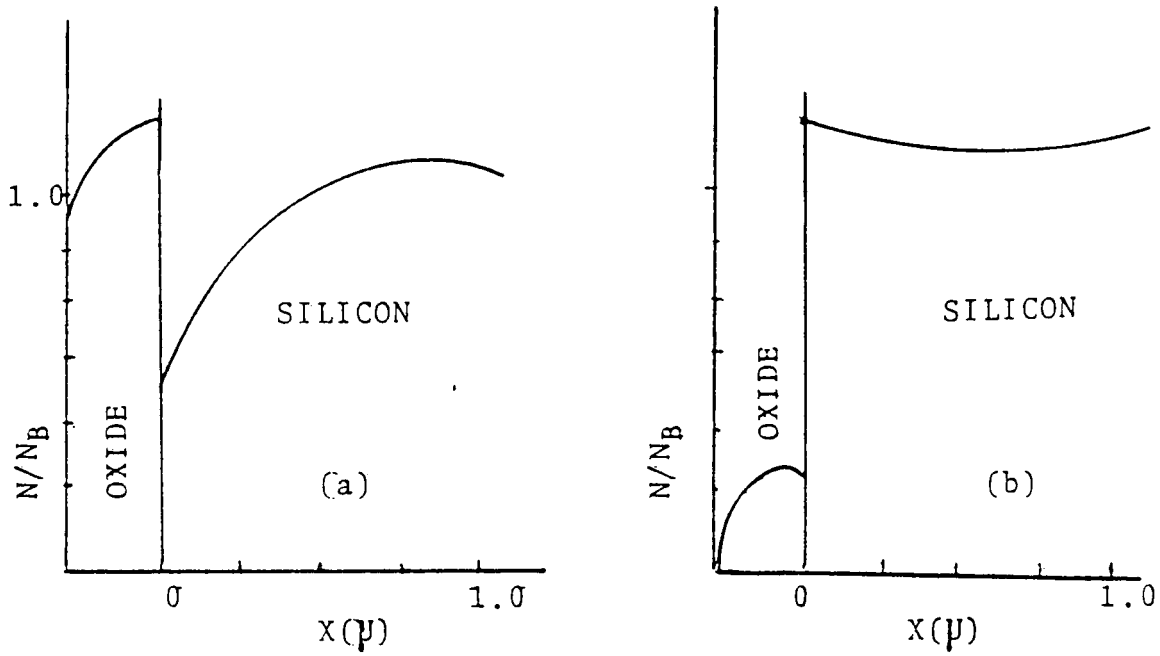


Figure 1.9 Redistribution of Boron and Phosphorous due to Thermal Oxidation

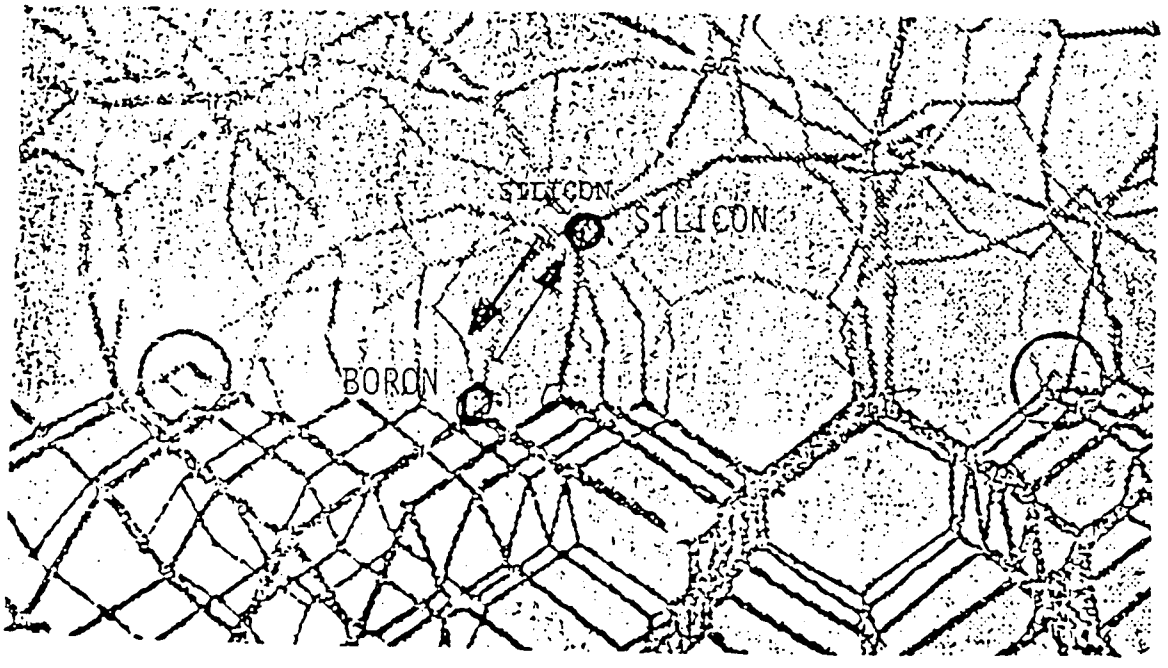


Figure 1.10 Boron Redistribution into the Oxide due to Radiation (From S.T. Pantelides [33])

Chapter II

CAPACITANCE-VOLTAGE MEASUREMENTS

The metal-oxide-semiconductor (MOS) capacitor with its associated capacitance versus voltage (C-V) curves is the simplest method for determining the electrical properties of the MOS system. Conductivity type, oxide thickness, flatband voltage and substrate doping density may be obtained from a single C-V curve and supplementary graphs [10, 11]. Using bias-temperature aging and a second C-V curve, other parameters such as flatband voltage shift, the number of mobile ions and presence of trapped charge may be determined. Deviations from the ideal curve also provide information about an MOS device's response to radiation.

2.1 CAPACITANCE VERSUS VOLTAGE CURVES

Capacitance versus voltage curves offer a nondestructive means of obtaining information about the three regions of interest in an MOS system--oxide, the Si-SiO_2 interface and the silicon. However, interpretation of the curves requires a basic knowledge of the ideal C-V curve.

The ideal C-V curve for an MOS capacitor of p-type bulk is illustrated in Figure 2.1. Normalized capacitance is plotted against voltage from accumulation through inversion. The capacitance of the MOS system may be described as two capacitors in series so that the total capacitance is equal to the capacitance of the oxide (C_{ox}) and the semiconductor capacitance (C_s) A surface charge versus surface potential plot, as well as charge and band diagrams are shown in Figure 2.2. Figures 2.1

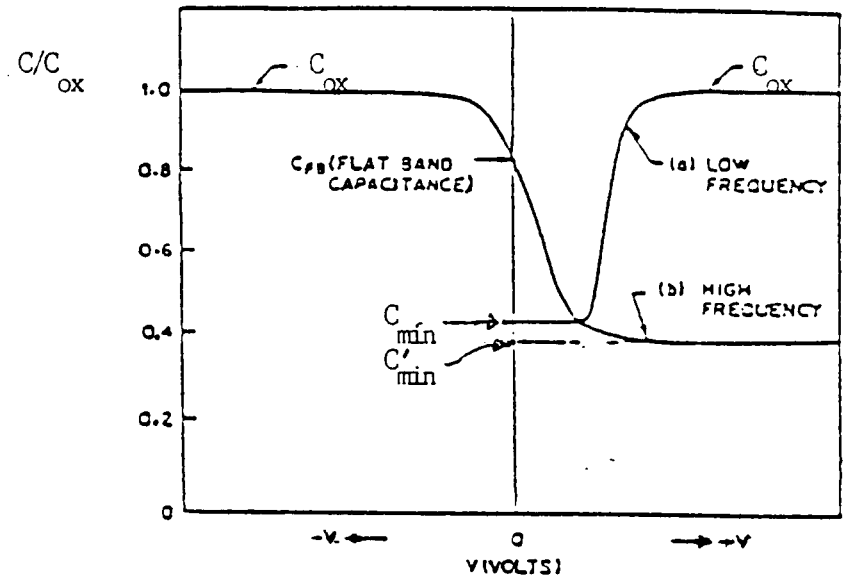


Figure 2.1 MOS Capacitance versus Voltage Curves (P-Type) (From Glaser/Subak-Sharpe [10])

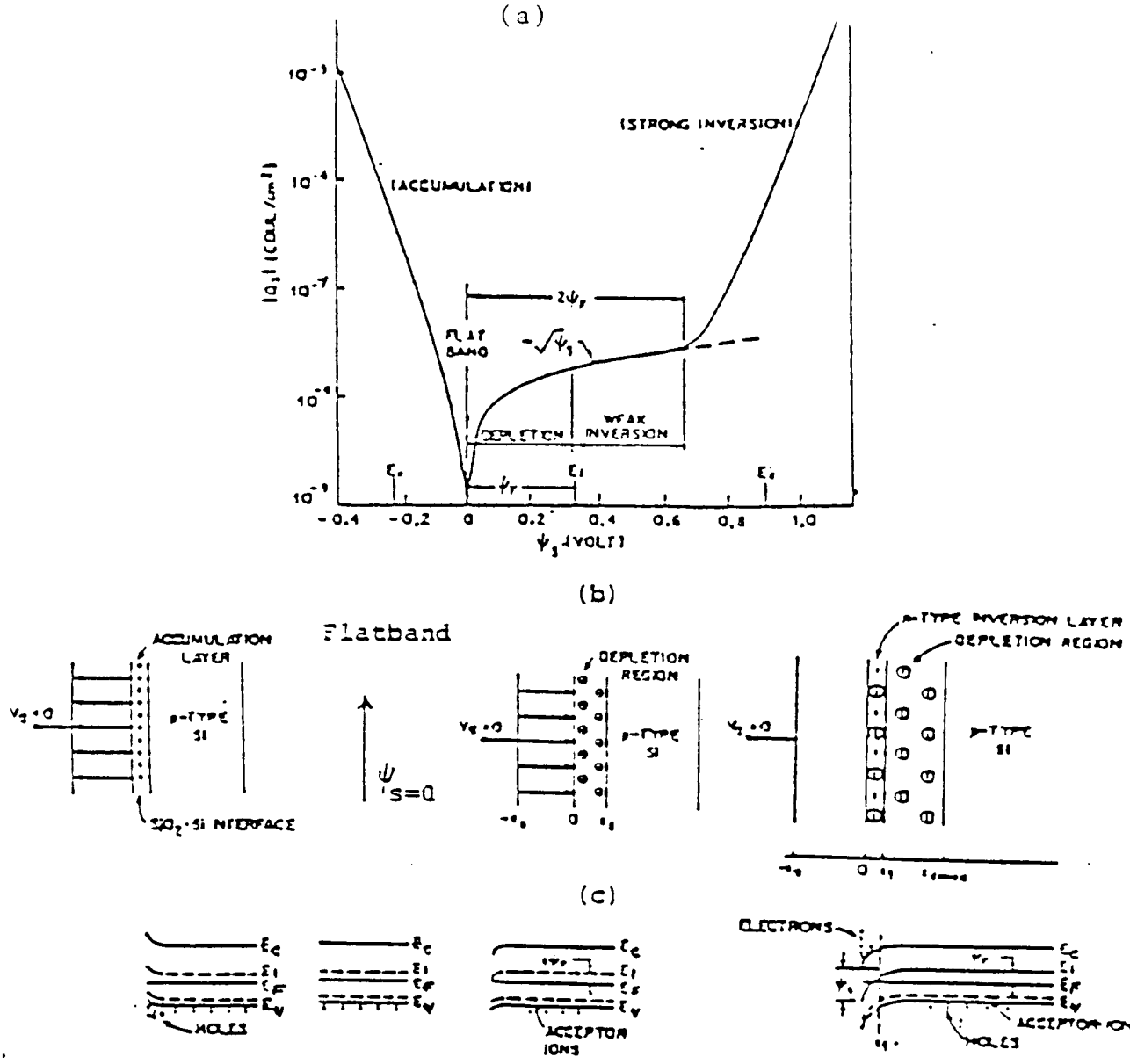


Figure 2.2 MOS Capacitance Response to Variation in Gate Potential

(a) surface charge as a function of surface potential

(b) charge distribution

(c) Energy band diagram
(From S.M. Sze [14])

and 2.2 will aid in the discussion on MOS capacitor response to varying gate potential. Only the p-type MOS capacitor is considered here although an analogous explanation exists for the n-type MOS capacitor.

When a negative voltage is applied to the capacitor ($V_G < 0$), positively charged holes (majority carriers) are induced at the Si-SiO_2 interface. The energy bands bend upwards such that the valence band is closer to the Fermi level. During accumulation, the MOS capacitor acts like an oxide capacitor.

For the unique case of $V_G = 0$, the capacitor is said to be at flatband. As indicated by its name, there is no band bending during flatband for there is no potential present to influence the charges, that is $U_S=0$.

As V_G becomes more positive, negative charge is induced near the silicon surface and majority carriers are repelled from the Si-SiO_2 interface, thus leaving behind uncompensated acceptor ions. The resulting width of uncompensated acceptor ions is called the depletion region. As more majority carriers are driven deeper into the semiconductor, the charge per unit area is decreased and hence the capacitance (C) decreases.

Weak inversion exists between $U_S = U_F$ and $U_S = 2U_F$. As V_G is made more positive, the depletion width almost reaches maximum value. Any additional negative charge goes into an inversion charge layer at the Si-SiO_2 interface. For the interval $0<U_S<2U_F$ (depletion and weak inversion), we obtain differential capacitance of the semiconductor space-charge region C_S.

$$C^{-1} = C_{ox}^{-1} + C_S^{-1} \qquad (2.1)$$

where:

C is total capacitance

C_{ox} is the capacitance of the oxide

C_s is the differential capacitance of semiconductor space charge region

Increasing the gate potential will yield values of U_s greater than $2U_F$ and the device is considered to be in strong inversion. Figure 2.2c illustrates that strong inversion is characterized by the band bending of the Fermi level E_F at the surface crossing the intrinsic Fermi level, E_i . thus causing a very thin n-type layer to form. The accumulation of minority carriers (electrons) at the Si-SiO_2 interface is sufficiently large enough to "invert" the surface. N-channel enhancement mode MOS transistors are normally off devices, but when inversion occurs, there is conducting surface layer and the device is thus on. The gate potential required to cause strong inversion is called the threshold voltage and is denoted by V_{TH}. At strong inversion, the depletion width reaches a maximum and the capacitance is minimum. In general, there are three types of C-V measurements: the high frequency method, the low frequency method, and a combined high-low frequency capacitance method.

2.1.1 HIGH FREQUENCY CAPACITANCE-VOLTAGE METHOD

The high frequency capacitance method can be used to determine interface trap density [12]. In this method, capacitance is measured as a function of gate bias with frequency

fixed at a high enough value so that interface traps do not follow the alternating current (ac) gate voltage.

The interface does follow slow changes in gate bias as the MOS device is swept from accumulation to inversion causing the high frequency C-V curve to stretch out along the gate bias axis because interface trap occupancy must be changed in addition to changing depletion layer charge. Fig 2.3 shows a hypothetical high frequency C-V curve, with the interface compared to an ideal C-V curve. The ideal C-V curve is calculated for the same doping density and oxide thickness but without interface traps. The curve with interface has been translated to cross the ideal curve at zero gate bias. Fig 2.3 also shows a shift in the C-V curve and a distortion in shape as a result of interface traps. The distribution of the interface traps level over the silicon band-gap does not affect the distortion.

At high frequency, the total capacitance is given by:

$$C_{hf} = C_s C_{ox}/(C_s + C_{ox}) \qquad (2.2)$$

where:

C_{ox} is the oxide capacitance per unit area.

C_s is the silicon capacitance per unit area.

The equivalent circuit shown in figure 2.4 corresponds to Equation 2.2. Since interface traps are not contained in Fig. 2.4, the high frequency capacitance of an MOS device will be the same as that of an ideal one without interface traps provided C_s is the same. However, C_s varies with band bending Qs, therefore C_{hf} will be the same if band bending Qs is the same. Knowing the

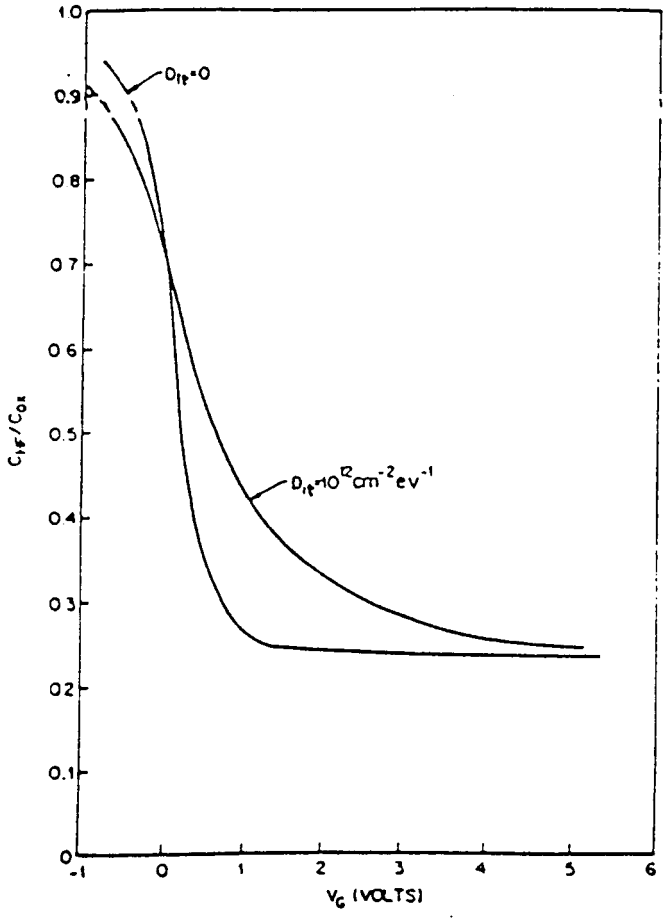


Figure 2.3 High Frequency Capacitance-Voltage Curve (From Nicollian and Brews [18])

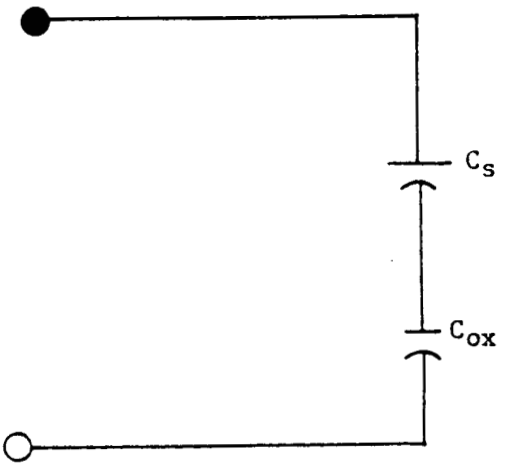


Figure 2.4 High Frequency C-V Equivalent Circuit

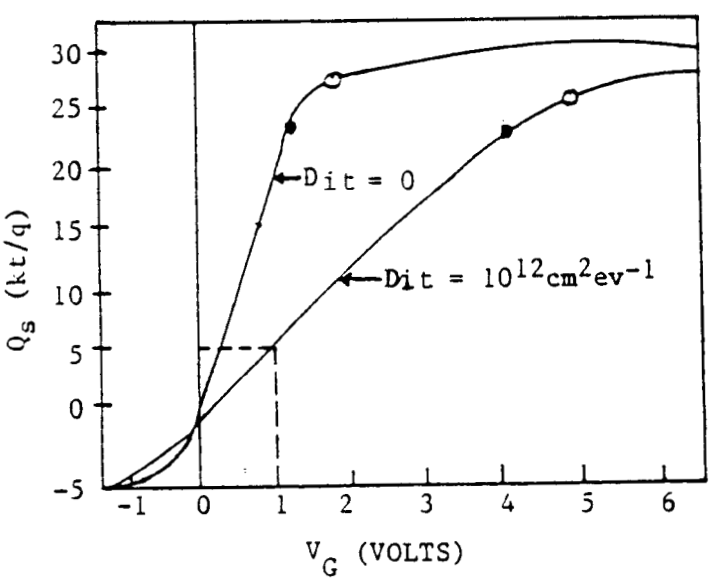


Figure 2.5 Surface Potential Versus Gate Voltage Curve
(From Nicollian and Brews [18])

Qs corresponding to a given C_{hf} in the ideal MOS capacitor, and measuring Vg corresponding to the same C_{hf} in the real capacitor, a plot of Qs versus Vg for the MOS with interface traps can be constructed. This Qs and Vg relationship contains all information about interface trap density at high frequency. Fig. 2.5 illustrates that interface traps stretch the Vs versus Vg curve along the gate bias axis. The amount of stretch out as measured by dVs/dVg determines the interface trap density (Dit). This can be obtained graphically or by numerical differentiation. The interface trap capacitance $C_{it}(Qs)$ can then be determined from:

$$C_{it}(Vs) = C_{ox} [(dVs/dVg)^{-1}] - C_s(Qs) \qquad (2.3)$$

$$C_{it} = q\ Dit \qquad (2.4)$$

C_{it} can also be read from a capacitance meter for a high frequency measurement. Dit is given as:

$$Dit = C_{it}/q$$

2.1.2 LOW FREQUENCY CAPACITANCE - VOLTAGE METHOD

The low frequency C-V method was first developed and used by Berglund [13]. The C-V curve in this case is measured at a frequency so low that the interface traps respond immediately to the ac gate voltage. This will contribute an additional capacitance C_{it} to the measured low frequency C-V curve. In addition, interface traps follow changes in gate bias so that the measured low frequency C-V curve will be stretched out along the gate bias axis like the high frequency method.

At low frequency, the total capacitance is given by:

$$1/C_{lf} = 1/C_{ox} + 1/[C_s + C_{it}] \qquad (2.5)$$

corresponding to the equivalent circuit shown in Fig. 2.6. This equivalent circuit shows that C_{it} can be extracted from the measured low frequency capacitance if C_s and C_{ox} are known.

$$C_{it} = [1/C_{lf} - 1/C_{ox}] - C_s \qquad (2.6)$$

To obtain C_{it} as shown above, one requires $C_s(Vg)$ calculated as a function of Vs involving doping profile. This calculation might lead to errors.

Berglund developed a method of obtaining Vs which is given by:

$$Vs = Vso + \int_{Vgo}^{Vg} dVg[\ 1 - (C_{lf}Vg/C_{ox})] \qquad (2.7)$$

The integrand is determined from a measured C_{lf} versus Vg curve. Vgo is an initial gate bias, corresponding to Vso.

With the experimental Vs versus Vg relationship established at the same low frequency, a derivative can be taken and used to obtain C_{it} (Vs), just as in the high frequency C-V curve, and Dit for low frequency curve is obtained.

Neglecting impurity redistribution will introduce error in Dit for both low and high frequency capacitance method. The redistributed profile with pile-up would result in a larger capacitance and delayed inversion compared to the uniform structure. When Dit is plotted as a function of band gap energy this error will not only affect the magnitude of Dit extracted at each energy but also the shape of the Dit versus band energy curve. In the case of the high frequency, and additional error

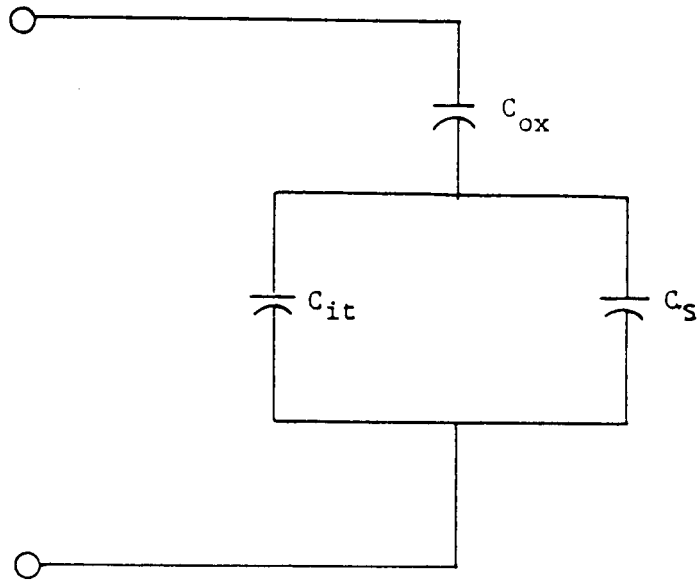


Figure 2.6 Low Frequency C-V Equivalent Circuit

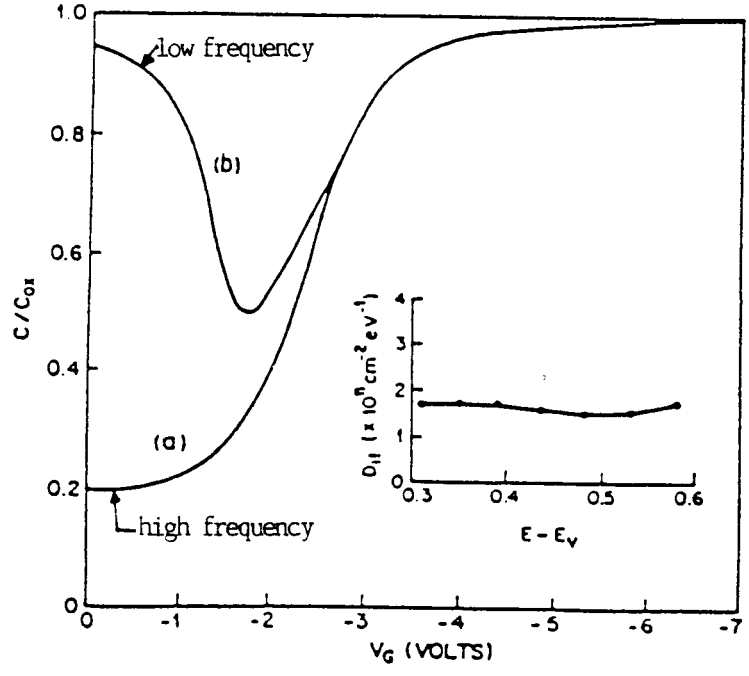


Figure 2.7 Combined High and Low Frequency C-V Curve (From Nicollian and Brews [18])

resulting from the differentiation, required to obtain Dit will be observed.

2.1.3 COMBINED HIGH-LOW FREQUENCY C-V METHOD

The combined high and low frequency capacitance method eliminates the need for the theoretical calculation of C_s and for the measurement of doping profile of the device.

From the high frequency equivalent circuit,

$$C_s = (1/C_{hf} - 1/C_{ox})^{-1} \qquad (2.8)$$

therefore the interface trap capacitance C_{it} will be equal to:

$$C_{it} = (1/C_{lf} - 1/C_{ox})^{-1} - (1/C_{hf} - 1/C_{ox})^{-1}$$

C_{it} is obtained directly from the measured C-V curve. Fig. 2.7 illustrates an example of C_{hf} and C_{lf} versus Vg given. At a given Vg, C_{ox} and C_{it} will be obtained from the curve, and Dit is determined from:

$$Dit = C_{it}/q$$

High and low frequency C-V are each obtained in different ways by sequential method or simultaneous method.

2.1.4 BIAS TEMPERATURE AGING

Bias temperature aging is a common reliability testing procedure where a device is heated while a voltage is applied to accelerate the failure processes. The standard bias-temperture test is briefly described below.

1. Measure the room temperature C-V curve.
2. Apply dc positive bias (desired field 1MV/cm)

3. Raise the temperature to 150^{o} - 300^{o} C.

4. Cool to room temperature.

5. Remove bias and measure another C-V curve.

6. Repeat step 2-6 for negative bias.

The shift in the C-V curve before and after bias temperature aging makes it possible to distinguish between mobile ions and radiation induced slow trapping.

2.1.5 DEVIATION DUE TO MOBILE ION CONTAMINATION

Ions of positively charged alkali metals are the most frequent oxide contaminants found in silicon wafer processing. Unlike other oxide charges, sodium ions are not restricted to any particular region in the oxide, but may be distributed throughout. The distribution of ions inside the oxide layer is illustrated in Figure 2.8 which shows that the greatest density (p) of mobile ions occurs at the two interfaces. Figure 2.9 indicates the locations of mobile ions and other oxide and interface charges. Of these ions, sodium is the most important because of its abundance in the environment and ease of mobility in SiO_2. Sodium may be introduced at a number of processing steps including: (1) gate or contact metallization, (2) oxidation and high temperature annealing, (3) high temperature processes such as diffusion and photoresist bake (4) chemical reagents used in cleaning, and (5) general handling of samples.

The positive charge of sodium ions cause the C-V curves to be displaced from the ideal curve along the voltage axis in the negative direction. Therefore, the resultant difference in

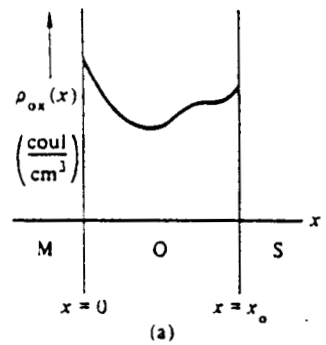


Figure 2.8 Distribution of Ions Inside the Oxide Layer (From R.F Pierret [11])

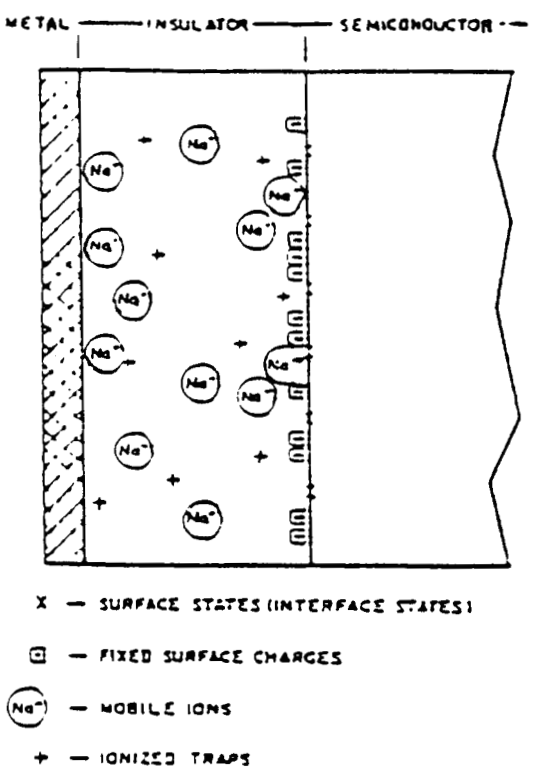


Figure 2.9 Charges in a Non-ideal MOS Capacitor (From S.M Sze [14])

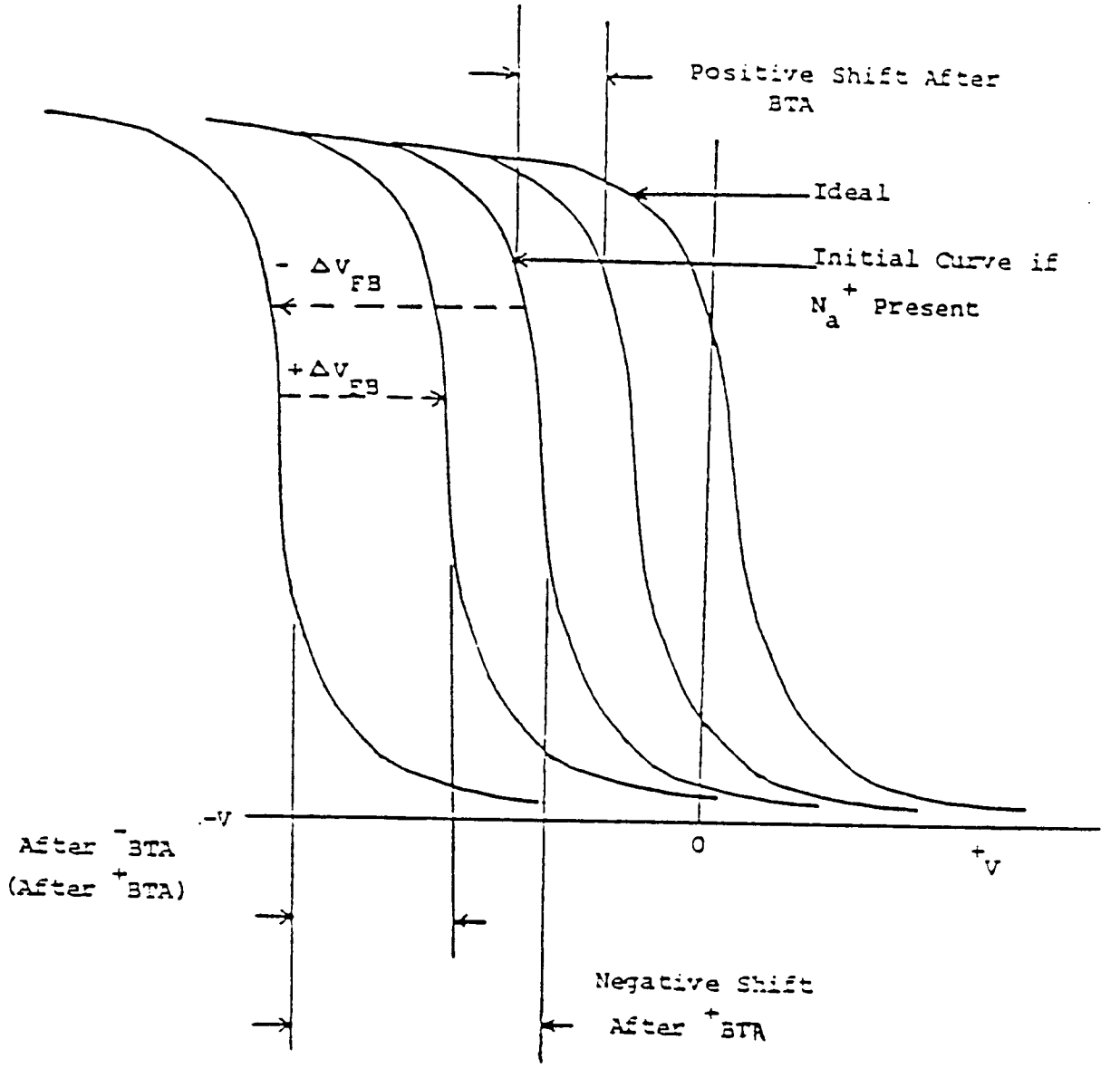
flatband voltage is negative. Negative mobile ions cause a positive shift in C-V characteristics. In addition to this initial shift in the C-V curve, other events occurred. Consider the following phenomena: (1) positive bias-temperature aging (150^{o} C) increased the negative C-V shift an additional tens of volts; (2) negative bias-temperature aging caused a positive shift in C-V characteristics. Figure 2.10 summarizes these observances. The flatband voltage shift between the C-V curve before and after bias-temperature aging is a measure or the mobile ion concentration drifted at the given temperature.

The events observed have been proven to be due to the sodium ions traveling between the two interfaces--metal-SiO_2 and SiO_2-semiconductor. Figure 2.11 shows the motion of positive and negative bias-temperature aging.

Control of mobile ion contamination has been accomplished through modification of the insulator such as the addition of phosphorus doping or the use of nitride barriers. Clean fabrication techniques are also employed to avoid contamination.

2.1.6 DEVIATION DUE TO RADIATION INDUCED TRAPPING

As stated earlier, the MOS capacitor is widely used in the study of radiation effects in SiO_2. Figure 2.12 illustrates the effect of ionizing radiation on the C-V characteristics of an MOS capacitor. Shown is a set of high frequency, C-V curves before radiation and after exposure to dosages of 6 $X10^{4}$and 2 X 10^{6} rads with +2.5 volts applied the gate. The C-V curves shift along the voltage axis to higher negative voltages, thus indicating that positive charge is being induced in the oxide as



BTA ≡ Bias Temperature Aging

Figure 2.10 Effect of Mobile Ions on C-V Curves

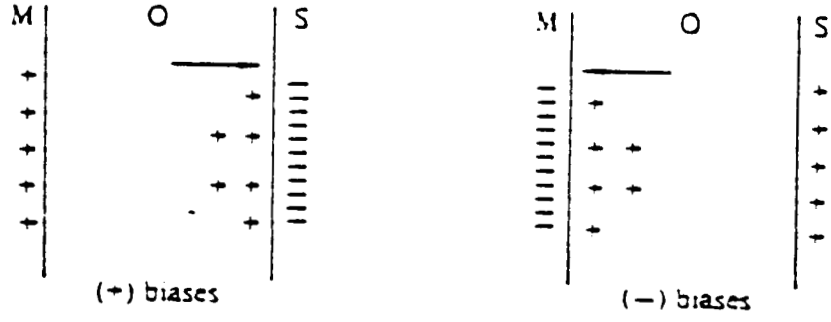


Figure 2.11 Effect of Positive and Negative Bias-Temperature Aging on Positive Mobile Ions
(From R.F. Pierret [11])

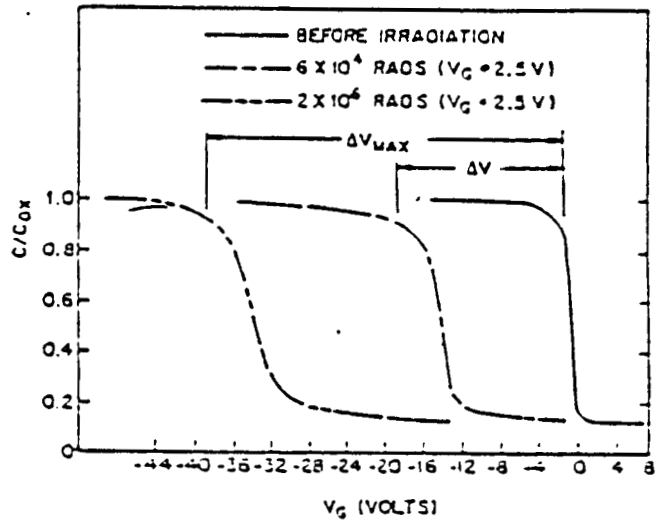


Figure 2.12 Deviation of C-V Curve Due to Radiation Induced Trapping
(From Nicollian and Brews [18])

a result of exposure to ionizing radiation. Also the induced positive oxide charge density increases with increasing radiation dose. In addition to the shift of the C-V curve along the voltage axis, the shape of the C-V curve is altered. After exposure to ionizing radiaton, the C-V curves are stretched out along the voltage axis. This voltage stretchout may be caused by an increase in interface trap level density.

The effect of ionizing radiation may be remedied by illumination with UV light or thermal anneal. Figure 2.13a shows percent annealing as a function of photon energy for four capacitors which have been irradiated with 3.4, 4.0, 4.5, and 5.0 eV photons. A +2V bias was applied during the irradiations. The abrupt rise in percent annealing is consistent with the Si-SiO_2 barrier energy of 4.25 eV. Electrons are injected from the silicon into the oxide conduction and subsequently neutralize the positive charge.

Figure 2.13b shows the results of the thermal annealing of p-channel MOSFETs with 1200 A gate oxides that had been irradiated with X-rays with +2V on the gate. The data shows that a device's threshold voltage can be restored to very near its original value with a high temperature anneal over long period of time.

2.1.7. DETERMINATION OF OXIDE THICKNESS

In order to determine the oxide thichkness from a C-V curve, the area of the dot (gate) must be known as well as the capacitance value during accumulation (C_{ox} or C_{max}). The oxide thickness may be calculated from Equation:

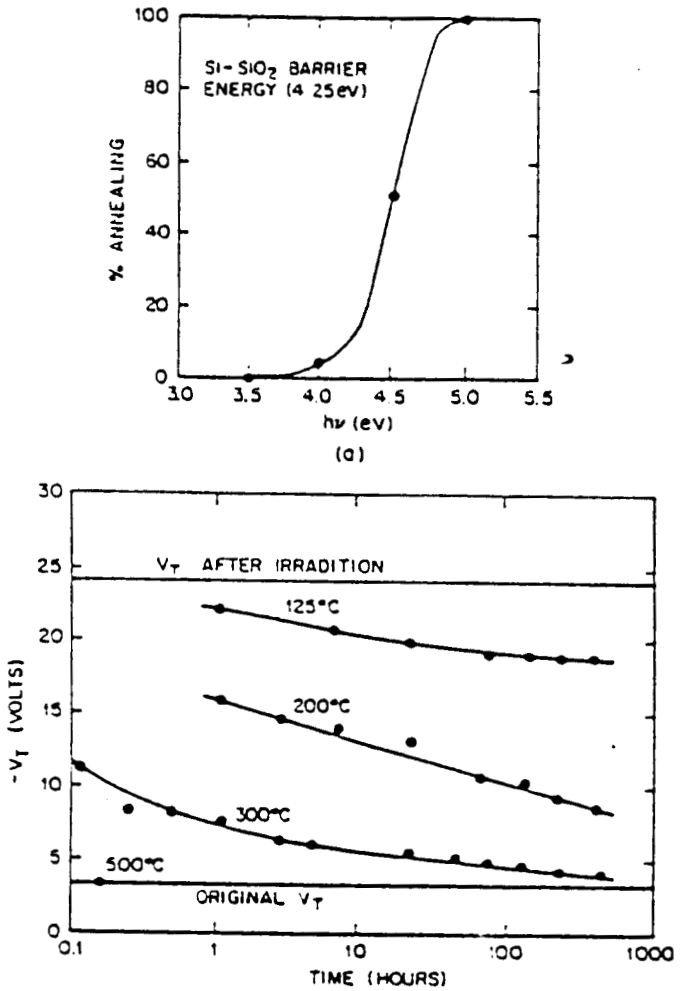


Figure 2.13 Annealing of Radiation Induced Charge

(a) Percent annealing as a function of photon energy

(b) Thermal annealing as a function of time and temperature
(From Nicollian and Brews [18])

$$x_o = (K_o \mathbf{E} A)/C_{ox} \qquad (2.9)$$

where:

x_o = oxide thickness (cm)

K_o = silicon dioxide dielectric constant (3.85)

$\mathbf{E}$ = permittivity of free space (8.85×10^{-14} farad/cm)

A = area of gate (cm)

C_{ox} = capacitance of the oxide (farad)

d = diameter of the gate (cm)

2.1.8 DETERMINATION OF FLATBAND VOLTAGE AND ITS SHIFT

The flatband voltage (V_{FB}) may be obtained by applying the value C_{min}/C_{max} from a C-V curve such as that found in Figure 2.14 to Figure 2.15 which shows C_{FB}/C_{min} for several values of oxide thickness. The C_{FB} value can then be applied to the original C-V curve and the corresponding V_{FB} evaluated. Suppose x_o = 1000 A and C_{MIN}/C_{MAX} = 0.23, then C_{FB}/C_{min} = 0.62. Since normalized capacitance is used, C_{max} is taken as one, and the corresponding voltage is -2.75 volts.

Flatband voltage shift (V_{FB}) may be determined by repeating the steps for determining flatband voltage and noting the difference between the two values of V_{FB}. Figure 2.14 shows a C-V plot for a p-type MOS capacitor before and after bias-temperature aging and the resultant flatband shift.

2.1.9 DETERMINATION OF THE SURFACE STATE LEVEL

Surface states have been shown to exist within the forbidden gap due to interruption of the periodic lattice structures at the surface of crystals. Historically, surface states have been

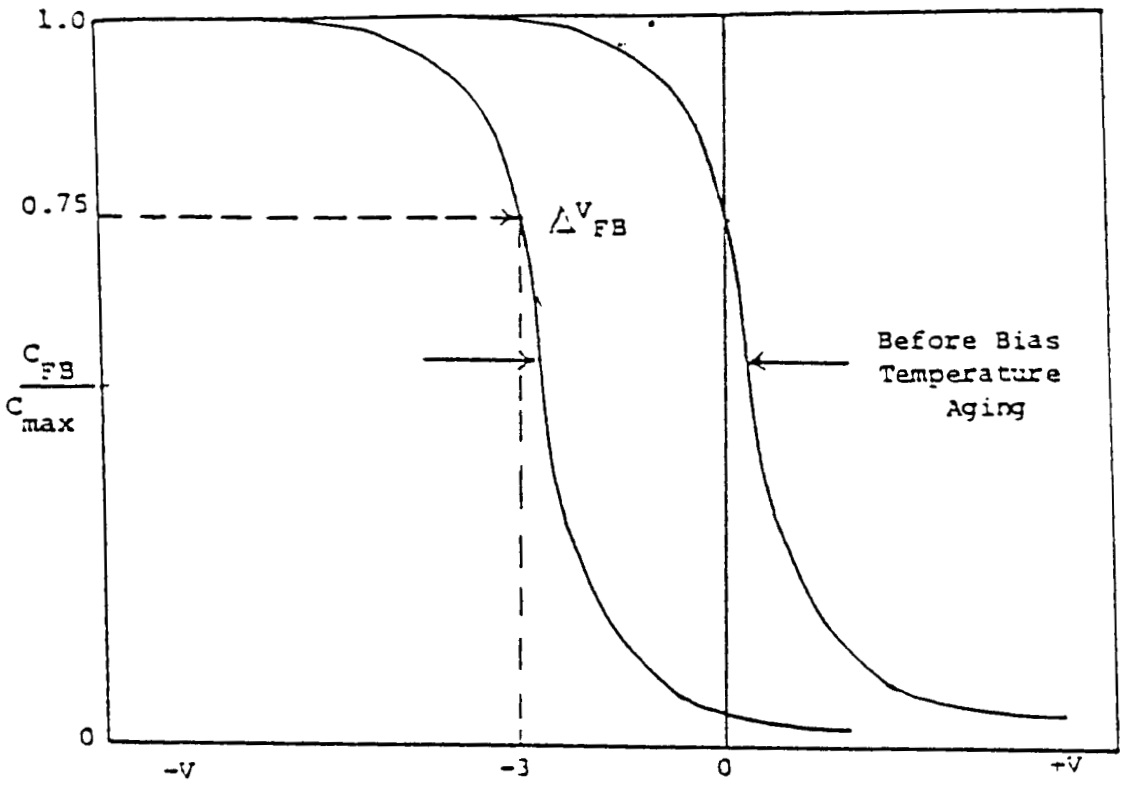


Figure 2.14 Normalized C-V plots of P-Type MOS Capacitor Before and After Bias-Temperature Aging

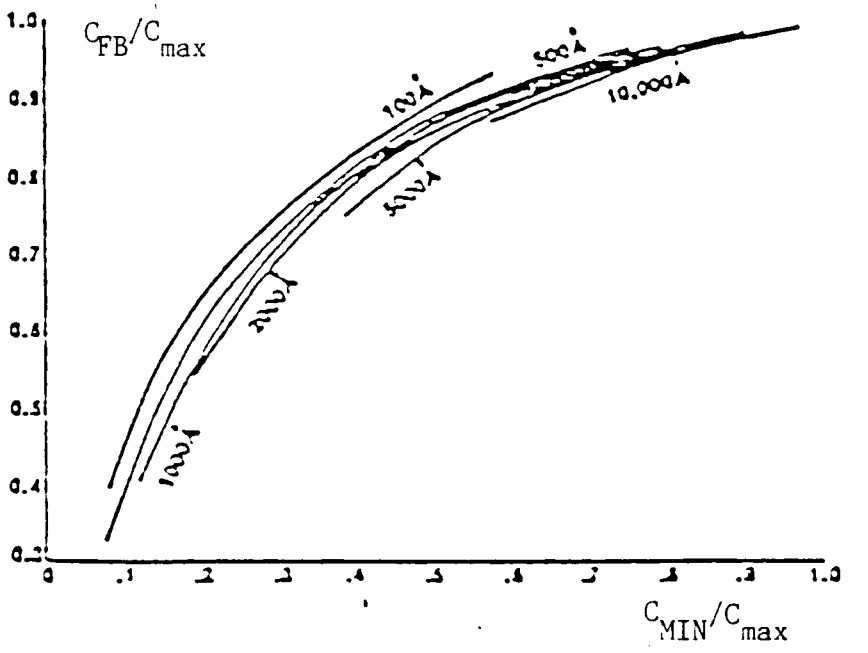


Figure 2.15 C_{FB}/C_{max} versus C_{min}/C_{max} for Several x_o

classified into fast and slow states. The fast states exchange charge with the conduction or valence band rapidly, and are assumed to lie close to the interface between the semiconductor and the insulator. Slow states, on the other hand, exist at least slightly away from the silicon-silicon dioxide interface and require a longer time for charge exchange.

A surface state is considered a donor state if it can be neutral or if it can become positive by donating (giving up) an electron. For an acceptor surface state, it can be neutral or it can become negative by accepting an electron. Interfacial traps in the upper half of the band gap are believed to be acceptor-like in nature. When a voltage is applied, the surface levels will move up or down with the valence and conduction bands while the Fermi level remains fixed. As the band bending is increased by an amount dUs, thus moving the conduction band edge toward the Fermi Level at the silicon surface (inversion in p-type substrate), the interface traps fill. The acceptor interface traps in the upper half of the band gap become negatively charged. This negative charge will contribute to a positive shift in MOS C-V curves and may contribute to the so called rebound effect.

To evaluate the surface state density one can use a number of methods (Terman analysis, Jeng analysis, etc.)[12]. However, the most practical method for this experiment, given the available instrumentation, was the differential capacitance method [14]. In the differential capacitance method, the capacitance is first measured at a high frequency. This yield

the high frequency curve shown in Figure 2.16 (dashed lines). The influences of the surface states on the voltage, however, cause a shift of the ideal MOS curve along the voltage axis. When surface states are present, the electric field in the oxide is higher than the field in the semiconductor surface, and more charges on the metal are necessary to create a given surface field in the semiconductor. Comparison of Figure 2.16 with the ideal MOS curve (figure 2.1) gives a curve of ΔV versus V where ΔV is the voltage shift. The total charge in the surface states (Q_{SS}) at a given surface potential is then given by [12]:

$$Q_{SS} = V_{FB}C_{OX} \quad (coul/cm^2) \qquad (2.10)$$

where:

Q_{SS} = surface state charge

C_{OX} = capacitance of the oxide

V_{FB} = flatband voltage shift

2.1.10 DISTINGUISHING BETWEEN MOBILE IONS AND TRAPPED CHARGE

In addition to identifying device parameters, the C-V technique can also be used to distinguish between various types of charges. Figure 2.17 illustrates how C-V curves and bias-temperature aging may be used to determine whether a charge effect is due to oxide fixed charge, mobile ions, or radiation induced slow trapping.

Once the bias-temperature aging steps have been carried out as outlined in Section 2.1.4, the resultant C-V curves may be used to characterize the type of charges involved. If after positive and negative bias-temperature aging, the curves are

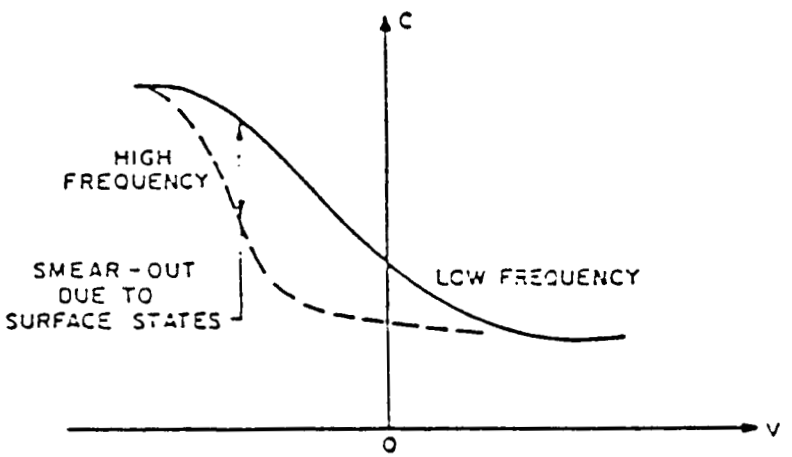


Figure 2.16 High-Frequency C-V Curve for P-Type Semiconductor (From S.M. Sze [14])

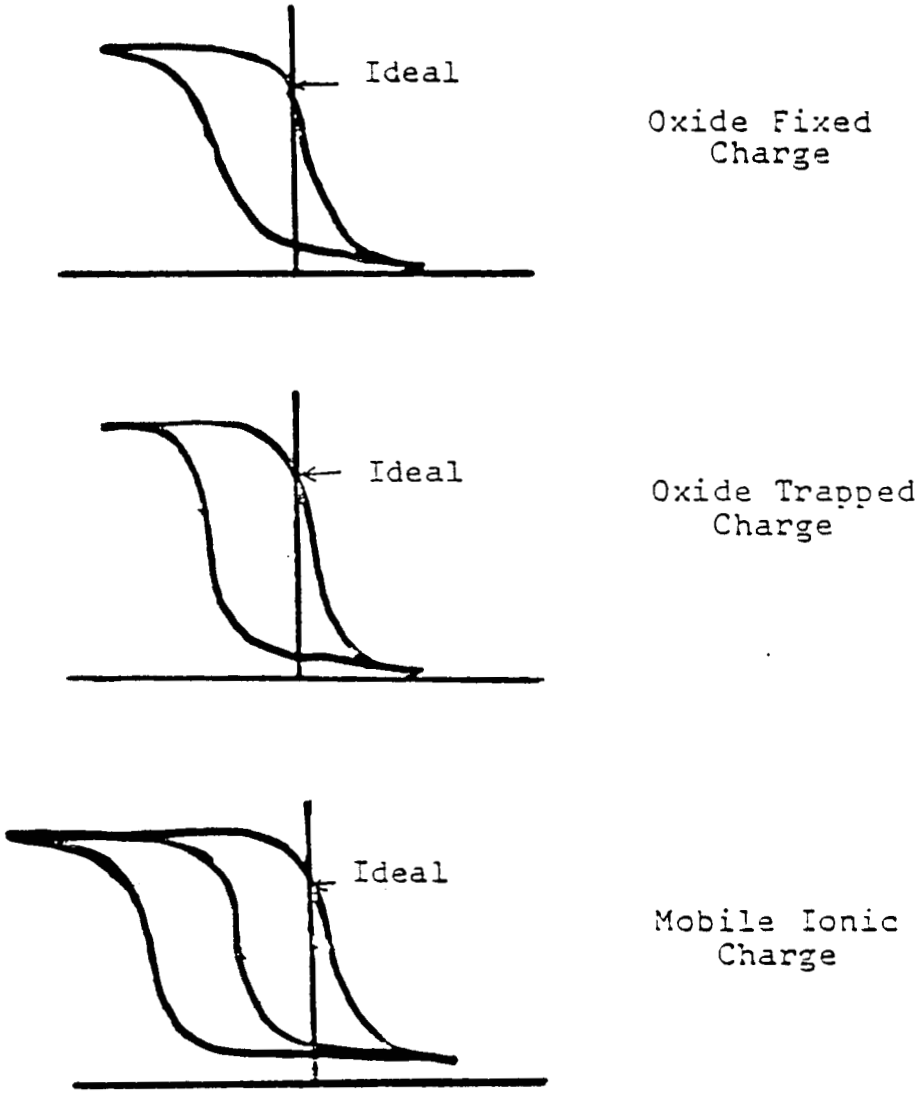


Figure 2.17 Distinguishing Between Oxide Fixed Charge, Oxide Trapped Charge and Mobile Ions

neither displaced along the voltage axis nor distorted, then only oxide fixed charge is present. It should be noted that the initial curve is already displaced from the ideal flatband voltage (zero volts) in a negative direction. This signifies that a positive charge has been induced.

If oxide positive trapped charge is present, bias-temperature aging will cause the curve to be shifted along the voltage axis in the positive direction regardless of the bias used. Negative and positive biasing will yield the same results.

Most activity is seen with mobile ions which move in both directions depending on the bias. Since sodium is the most commonly encountered mobile ion, the initial curve is shown with its flatband voltage shifted in the negative direction with respect to the ideal flatband voltage. On positive bias-temperature aging, the C-V curve shifts more negatively. Negative bias temperature aging then causes the curve to shift in a positive direction back to its original position. Mobile ions were also discussed in Section 2.1.5.

2.2 EXPERIMENTAL TECHNIQUES

2.2.1 SAMPLE PREPARATION

The MOS capacitors used in this part of the work were supplied by AT&T Bell Laboratories. The (100), p/p+ wafers, were initially given a sulfuric peroxide clean, an ammonium hydroxide clean and a 15:1 H_2O:HF clean (30 seconds). Next, 6000 A of undoped polysilicon was deposited using low pressure chemical vapor deposition (LPCVD) with a hydrochloric acid flush. The LPCVD was followed by a phosphorus predeposition at 950^{o}C. After

removing the phosphorous glass with a 15:1 H_2O:HF clean (2 minutes), the samples were checked for a sheet resistance of approximately 10^{-3} ohms/square. The samples were then given a 900°C nitrogen anneal and a 500° C hydrogen bake. A two minute 15:1 H_2O:HF clean was followed by magnetron sputter depostion of one micron of aluminum (aluminum-copper-silicon) to form the front contact. The ring dot pattern was formed using photoresist, a ring dot mask and an aluminum wet etch. A special polysilicon etch (10-6-1 nitric-acetic-HF) was followed by a fresh J-100 resist strip. One micron of aluminum was then applied to the back side by thermal evaporation. The final step was an aluminum sinter at 450° C in hydrogen.

2.2.2 INSTRUMENTATION

The apparatus used for the C-V measurements is shown in the block diagram of Figure 2.18. The end products of the instrumentation depicted included a C-V plot and a computer print-out of the maximum and minimum capacitance and voltage values, the flatband capacitance and voltage, the oxide thickness, the doping density, the density of surface states and an average of most of these values.

The HP 7004B X-Y Recorder graphically displayed the capacitance and voltage values. The HP 3478A Multimeter digitized the analog current and voltage readings coming from the C-V plotter. The Multimeter allowed values to be more easily read than they would have been were the graph alone used. Since the system was only semi-automatic, it was important to be able

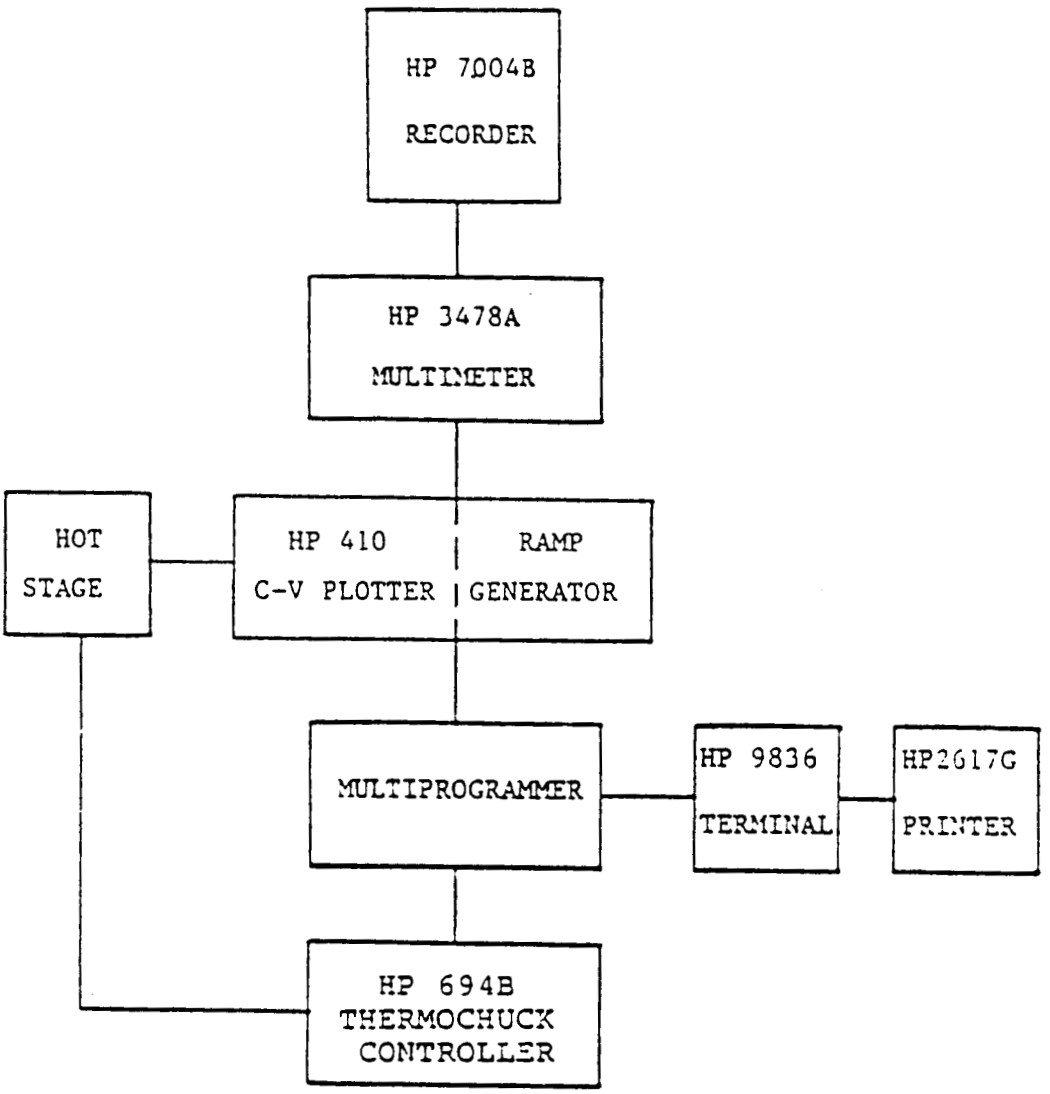


Figure 2.18 C-V Bias-Temperature Aging Apparatus

to identify certain fluctuations in voltage.

The key instrument in the C-V measurements was the HP 410 C-V plotter and its built-in ramp generator. The Plotter performs the capacitance and voltage measurements while varying the applied voltage with the ramp generator.

Coordination of instrumentation and sampling of data was the task of the Multiprogrammer. The Multiprogrammer alternately sampled capacitance and voltage measurements from the C-V plotter and supplied the values to the HP 9836 Computer Terminal where they were stored and used in other calculations. The computer program used for the C-V bias-temperature aging measurements assumes a metal-semiconductor work function value of 0.07V. However, the experimental range of the work function is within 0.02V of this value. The accuracy of flatband voltage with this instrumentation is within 0.01 V. The computer program used to calculate the desired parameters was written by Sharon Knotts [9].

Bias-temperature aging experiments were made possible with the aid of an HP 6940B Thermochuck and a custom-built hot stage The Thermochuck enables the user to heat and cool samples as desired for bias-temperature aging experiments. Automatic and manual operation is possible. Samples were heated on a hot stage. In addition to the hot stage, the heating unit was also equipped with three probes for electrical characterization, a vacuum to secure the wafer on the stage, and a light for injection studies.

Direct oxide thickness measurements were performed using an Automatic Ellipsometer and a Nanospec Model 010-0180. The

Ellipsometer is a precision optical instrument which measures changes in the state of polarized light reflected from the surfaces of the samples. The Nanospec is a computerized thickness measurement instrument based on tne principles of reflective spectroscopy. The Nanospec uses an internal calibration based on assumed values of refractive index for each film type desired.

The Sherman Fairchild Van de Craaff Accelerator can produce, in air, a beam of high energy electrons whose knetic energy can be set between 1 and 3 MeV. The kinetic energy of the irradiating electrons for this experiment was 2 MeV.

2.2.3 EXPERIMENTAL PROCEDURE

Freshly obtained samples were measured for oxide thickness with AT&T ellipsometer and Nanospec and verified with Prairie View A&M University Nanospec. Average thickness values of 884 Å and 997 Å were obtained for waters SIF 56-370 and SIF 56-185 respectively (Table 2.1). The values obtained with the ellipsometer and Nanospec were slightly lower than those obtained with the C-V curve because the polysilicon etch slightly attacked the gate oxide.

Capacitance versus voltage curves were then obtained for both wafers at room temperature. Maximum and minimum capacitance and voltage, flatband capacitance and voltage, oxide thickness, doping density, density of surface states and the averages of some of these parameters were computed and recorded. No bias was applied to the wafers during this initial measurement.

TABLE 2.1 OXIDE THICKNESS MEASUREMENTS

INSTRUMENT	SIF 56-370	SIF 56-165
AT&T Nanospec	883 Å	999 Å
AT&T Ellipsometer	884 Å	994 Å
PVAMU Nanospec	886 Å	997 Å
C-V Curve	956 Å	1030 Å

Specifically, dots (3,4), (6,4) and (6,5) or wafer SIF 56-370 were chosen for measurement. Also selected were dots (3,3), (6,6), and (9,8) of wafer SIF 56-185.

The samples were then checked for mobile ion contamination using bias-temperature aging as outlined in Sections 2.1.4. Although a significant flatband voltage shift (-0.23V) was observed when the samples were positively bias-temperature aged, an insignificant flatband voltage shift (< -0.01V) was observed after negative bias-temperature aging. Had the flatband voltage shift (V_{FB}) been due largely to mobile ions, a comparable V_{FB} would have been observed using negative bias temperature aging. Therefore, it was concluded that the samples were, for experimental purposes, free of mobile ions and that other factors accounted for the shift during positive bias-temperature aging. A slight increase in Qss could be evidence of slow trapping due to unannealed sputtering contamination. Hysteresis was observed which may be indicative of some acceptor state charging during inversion. However, we cannot distinguish N_{it} from Dit or separate Qss into Q_{it} and Q_f.

The Sherman Fairchild Van de Graaff accelerator was used to irradiate both samples with 2 MeV electrons. The wafers were cut to allow irradiations of different dosages to dots on the same wafer. Dot (3,4) of SIF 56-370 was irradiated 24 seconds (19.3 krad). The top half was then removed and the bottom portion of the wafer (dots (6,4) and (6,5)) received an additional 5.3 krad (7.1 seconds) for a total dosage of 24.6 krad. Irradiation times were computed using the equation:

$$t = rad/803.81 \qquad (2.11)$$

where:

t = length of time irradiation (sec)

rad = desired irradiation dosage

Following irradiation, sample SIF 56-370 was measured at room temperature with a 2MV/cm field applied. After an overnight anneal (4.2×10^4 - 5.2×10^4 seconds) at room temperature and a 2 MV/cm field, the sample was remeasured. Final measurement took place after positive bias-temperature aging at 250° C for 15 minutes with a 2MV/cm applied field.

A similar procedure was used with wafer SIF 56-185 except the radiation doses were changed and the samples were heated overnight at 137° C. The radiation doses were 15 krad (18.66 seconds) for dot (9,8) and 25 krad (31.1 seconds) for dots (3,3) and (6,6). Figure 2.19 outlines the experimental procedure for both wafers.

2.3 EXPERIMENTAL RESULTS AND DISCUSSION

The initial test for mobile ions eliminated mobile ions as a probable cause of flatband voltage shifts. The shifts experienced were therefore concluded to be due to interface states, rebound or oxide trapped charge.

Since a time difference existed between the times that the two lots were measured following irradiation, measurements were extrapolated back to 100 seconds after irradiation. It was assumed that V_{FB} change in the period immediately following irradiation was governed by hole transport. Ideally, this step

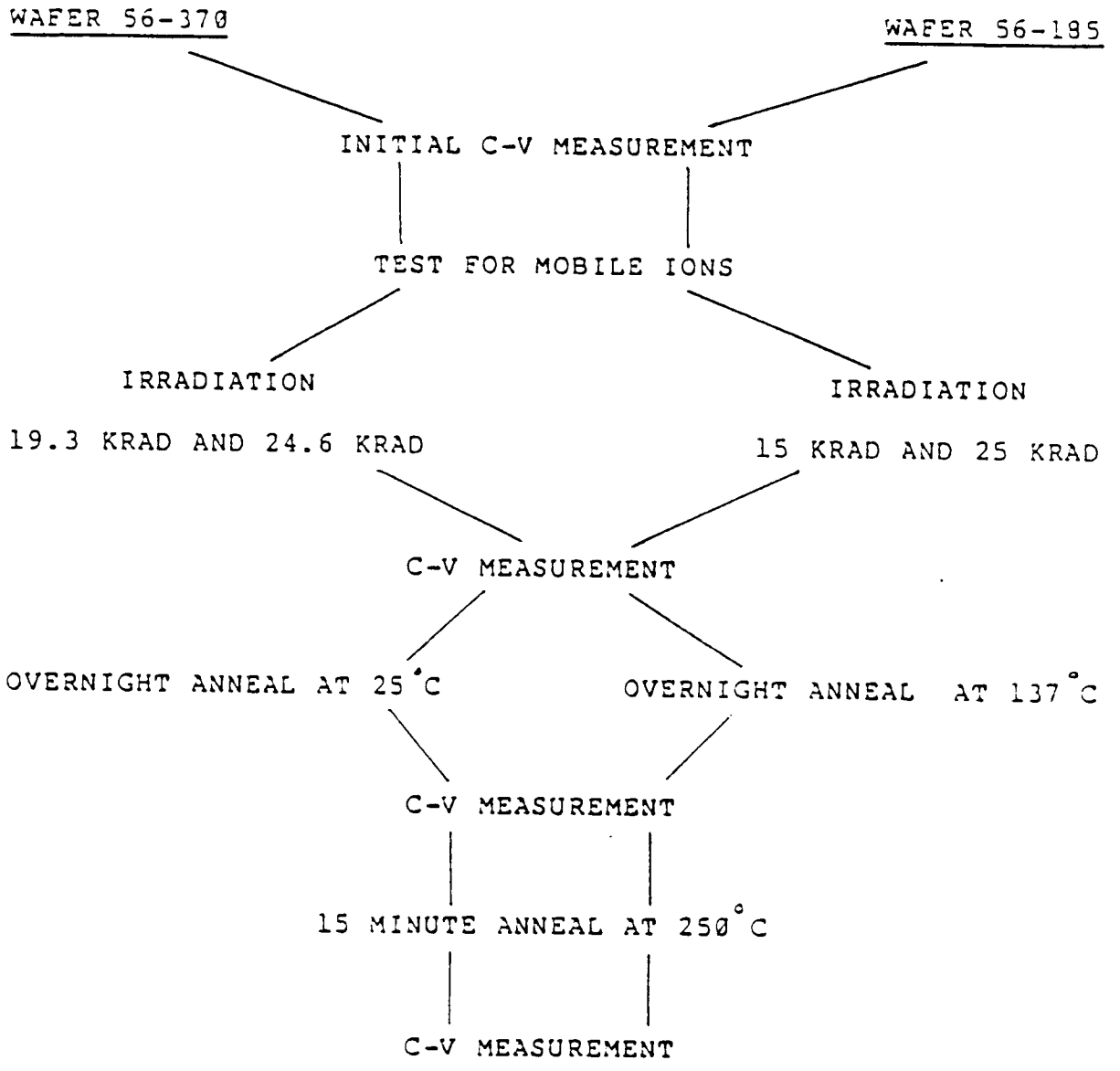


Figure 2.19 Experimental Flow Chart

would have allowed easier comparison of values. To perform the extrapolations, the Einstein relation given in Equation (2.12) was used.

$$D/u = K\ T/q \qquad (2.12)$$

where:

D = diffusion coefficient

u = mobility of holes in SiO_2

K = Boltzman constant

T = temperature in degrees Kelvin

q = magnitude of electronic charge

Nicollian's model [18] for creation of hole-electron pairs requires hole transport through the SiO_2. If hole transport is controlled by bulk oxide traps, the times that holes spend in these traps are spread over a wide range and comparable to the transit time of the holes across the oxide. Consequently, the transit time, t_T increases more rapidly than linearly with oxide thickness, x_o. The customary mobility, $u = x_o/t_T F_{OX})$, (where F_{OX} is the oxide field) is then oxide thickness dependent, field dependent and time dependent. The mobility has been experimentally determined to be 1.2×10^{-2} exp(-0.16q/Kt) and therefore the mobility at room temperature has been stated to be 2.0×10^{-5} cm^2 /V-sec. The diffusion was calculated from the Einstein relation and is 5.31×10^{-2} cm /sec. The relationship: given in Equation (2.13) was used to extrapolate the values back to 100 seconds after irradiations.

$$x/n = \sqrt{D\ t_n}/\sqrt{[D\ t_x]} \qquad (2.13)$$

where:

x = unknown voltage due to radiation dosage

n = known voltage due to radiation dosage

D = diffusion coeffient

t_n = length of time in seconds between time of irradiation and time of measurement of sample with known voltage.

t_x = length of time in seconds between time of irradiation and time of measurement of sample with known voltage.

Table 2.2 summarizes the post irradiation values. As mentioned earlier, attempt was made to extrapolate these values to a common point. However, inconsistent results were obtained which could be accounted for by discrepancies in the radiation doses received on different days.

The initial measurements following irradiation displayed the characteristic negative flatband shift and increase in Nss. Tables 2.3 and 2.4 give some typical values for both SIF 56-370 and SIF 56-185. Extrapolated values point to an immediate after irradiation flatband voltage of approximately -6V. Mitchell's investigation [18] (Figure 2.20) indicates that -7V is a more reasonable value for 25 krad irradiation with +10V bias during irradiation. Overnight annealing even at room temperature was shown to be significant. The 250° C quick anneal improved V_{FB} even more.

Looking at the graphical presentation of data the (Figures 2.21 and 2.22), it is easy to see that the charge neutralization of oxide trap; and N_{ot} and possibly interface face trap annealing is

TABLE 2.2 Statistical Summary of Experimental Data

		SIF 56-370	SIF 56-185
1.	Average Initial V_{FB} (volts)	-0.80	-0.78
2.	Average Initial N_{SS} (cm^{-3})	3.36×10^{10}	5×10^{10}
3.	Average V_{FB} after 25 krad	-1.68 (4200s)	-3.08 (5100s)
4.	Average N_{SS} after 25 krad	3.27×10^{11} (4200s)	5.78×10^{11} (5100s)
5.	Average V_{FB} after 25 krad (Pre-+Bias	-0.89	-----
6.	Average N_{SS} after 25 krad (Pre-+Bias	1.50×10^{11}	-----
7.	Average V_{FB} after overnight anneal	-1.54 ($27^{o}C$)	-1.46 ($137^{o}C$)
8.	Average N_{SS} after overnight anneal (approx. 45,000s)	2.99×10^{11} ($27^{o}C$)	2.45×10^{11} ($137^{o}C$)
9.	Average V_{FB} after quick anneal (900s)	-0.54 ($250^{o}C$)	-0.78 ($250^{o}C$)
10.	Average N_{SS} after quick anneal (900s)	7.0×10^{10} ($250^{o}C$)	1.02×10^{10} ($250^{o}C$)

* NOTE: Inconsistencies Present in Data. Greater differences observed in the 15 krad irradiation than in the 25 krad irradiation in some instances. Actual radiation dos was probably not the expected radiation dose.

TABLE 2.3 TYPICAL DATA: LOT SIF 56-370

	V_{FB} VOLTS	N_{SS} (cm^{-2})	V_{FB} VOLTS	N_{SS} (cm^{-2})
Initial Measurement; Room Temperature; No Bias	-0.79	5×10^{10}	---	---
Post Irradiation (25 Krad) Time Lapse: 5400s Room Temperature; 2Mv/cm	-2.62	4×10^{11}	1.88	3.5×10^{11}
Overnight Anneal - 45000s Room Temperature; 2MV/cm	-2.45	3.7×10^{11}	0.17	-3×10^{10}
Quick Anneal - 900s 250°C; 2MV/cm	-1.43	1.39×10^{11}	1.02	-2.31×10^{11}

TABLE 2.4 TYPICAL DATA: LOT 56-185

	V_{FB}(V)	$N_{SS}(cm^{-2})$	V_{FB}(V)	$N_{SS}(cm^{-2})$
Initial Measurement; Room Temperature No Bias	-0.72	5×10^{11}	---	---
Post Irradiation; 25 Krad Time Lapse; 4200 seconds Room Temperature	-3.81	6.3×10^{10}	-3.09	5.8×10^{10}
Overnight Anneal Time Lapse: 45:00 seconds 137°C	-2.2	2.92×10^{11}	1.61	-3.38×10^{11}
Quick Anneal Time Lapse: 900 seconds 250°	1.52	1.49×10^{11}	0.68	-1.43×10^{11}

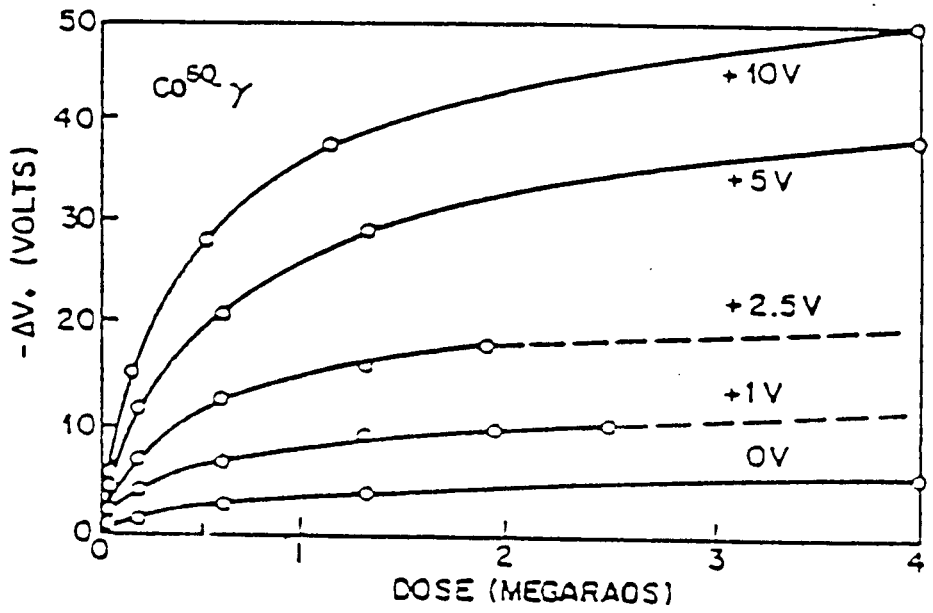


Figure 2.20 Flatband Voltage Shift versus Radiation Dose for Various Biases (Form Nicollian and Brews [18])

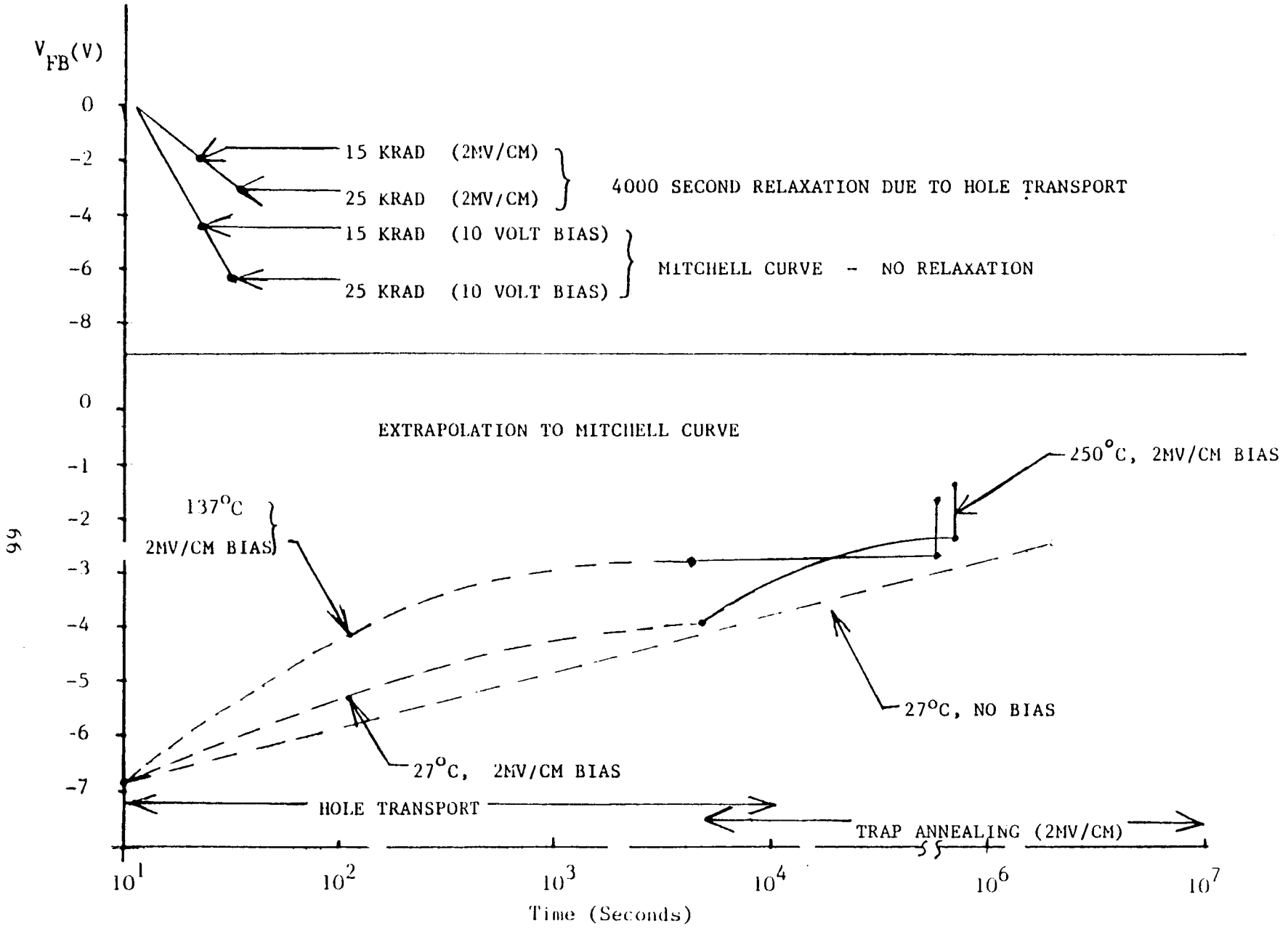


Figure 2.21 Annealing Processes: V_{FB} versus Time

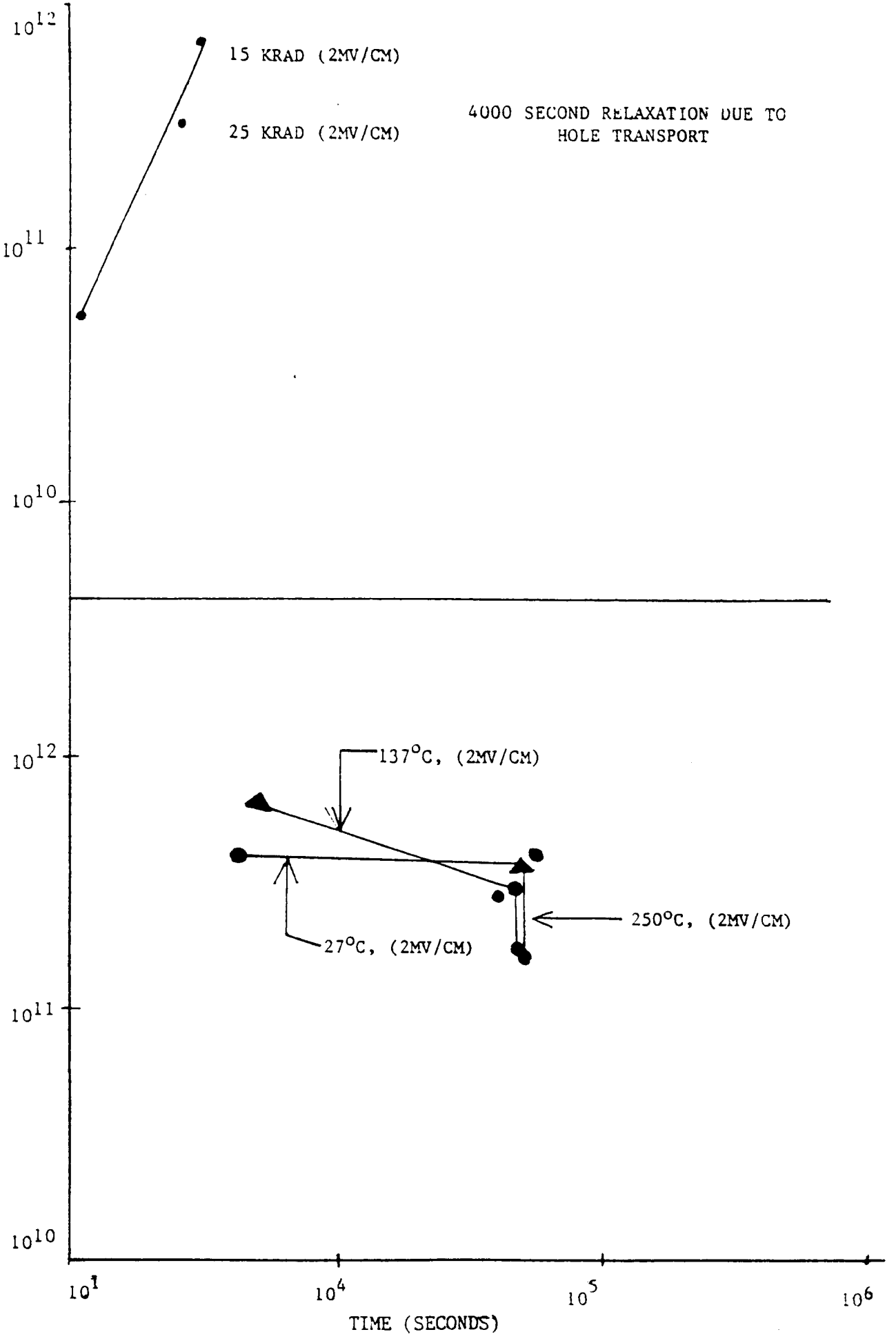


Figure 2.22 Annealing Processes: Nss versuss Time

strongly dependent on temperature. Flatband voltage values have been extrapolated back to Mitchell's -7.0V value as mentioned above. Regions of rapid hole transport and V_{Not} are also shown. Using extrapolated values, and activation energy of 0.12eV was calculated. Winokur [15] reported an activation energy for annealing processes as 0.41eV.

Annealing of oxide traps may occur by: 1) charge neutralization (injection of electrons to neutralize a charge) or 2) trap removal. It is interesting to note that a simple Arrhenius plot could not be drawn for the annealing curve of Figure 2.13b. Therefore, there is reason to suspect that the annealing process is not a single mechanism, but perhaps several mechanisms. This is confirmed by the V_{FB} annealing versus photon energy curve (Figure 2.13a) which shows that in order for effective annealing to occur, the Si-SiO_2 energy barrier must be exceeded. Winokur [16] reported better annealing in polysilicon-gated material than in aluminum-gated material.

An interesting phenomena was observed in samples that had been pre-positively biased. These samples showed some degree of radiation resistance. Note the lessened effect on flatband voltage and Nss which are indicators of radiation damage. Samples that had been pre-positively biased had an average V_{FB} of -0.89V while those that had not been pre-positively biased had an average V_{FB} of -1.68V. Average increases in Nss values were 1.5×10^{11} for pre-positively biased samples compared to 3.2×10^{11} for samples not pre-positively biased.

No substantial N_{it} effect due to acceptor interface trap

filling (negative charge at the Si-SiO_2 interface) was observed. Measurement of N_{it} was not possible with the instrumentation used. Had V_{Nit} been significant, a large net effect on the V_{FB} would have been observed. It is also interesting to note that Winokur [16] actually measured two types of interface traps and hence Dit and not N_{it} (which is based on only one type of charge carrier) was measured. In contrast to Winokur who claimed that no significant Nss changes occurred during anneal, this study showed continued flatband voltage and Nss recovery in the damaged capacitors during both the room temperature anneal and the 137° C anneal.

A mechanism proposed by T.N. Fogarty and S. Knotts may explain the increased rebound due to negative charging at the Si-SiO_2 interface in p-type polysilicon-gated samples. The greater rebound may be nothing more than increased hydrogen content in SiO_2 and its interaction with the SiO_2 network at the interface in polysilicon-gated devices. Polysilicon is deposited by thermal decomposition of silane, thereby increasing hydrogen content immediately below the gate in SiO_2 and resulting in fuller rapid anneals as discussed by Aitken [17].

Considering the network theory of glasses in a p-type material, the events leading to annealing of interface traps may proceed as follows. Hydrogen diffuses from under the gate to the Si-SiO_2 interface. Introduction of boron into the predominantly SiO_2 network causes one oxygen atom to be freed from the network for each two silicon atoms replaced by two boron atoms. Now hydrogen added to the system can combine with the free oxygen and form hydroxyls which may account for negative charge at the

interface and produce the rebound effect. Thus hydrogen at the SiO_2 interface may possibly form hydroxyls at the $Si-SiO_2$ interface or repair dangling bonds at the same interface. Therefore, the formation of hydroxyls would be more probable in a boron doped silicate as it would require only the energy necessary to form the O-H bond.

In intrinsic silicon or in phosphorous doped n-type silicon systems where phosphorous could act as a deoxider to the SiO_2 network, the replacement of two silicon atoms with two phosphorous atoms ties up excess oxygen. Therefore, in contrast to p-type material, all hydrogen added to the system goes toward the repair of dangling silicon bonds at the Si-SiO2 interface.

Chapter III

CHARGE PUMPING MEASUREMENTS

3.1 THE CHARGE PUMPING PHENOMENA

Charge pumping is a well-established technique for the determination of surface state density in metal-oxide-semiconductor transistors. This technique has the advantage of being applicable for transistors with small gate area, a situation for which the C - V measurement technique cannot be used.

This technique was introduced by Brugler and Jesper [19]. It is based on a recombination process at the silicon-silicon dioxide interface involving the surface states. This induces a substrate current which can be directly related to the surface state density. Since then, different models have been presented using this technique to determine the surface states density [20, 21]. This work will investigate some of the models experimentally, taking into account the emission of holes and electrons to the valence band or the conduction band respectively, depending on the state of $Si-SiO_2$ interface.

3.1.1 BASIC PRINCIPLES

The basic experimental set up, as introduced by Brugler and Jesper [19], is illustrated in Fig. 3.1 for an n-channel transistor. The source and the drain of the transistor are connected together and held at a certain reverse bias voltage with respect to the substrate. When the transistor is pulsed

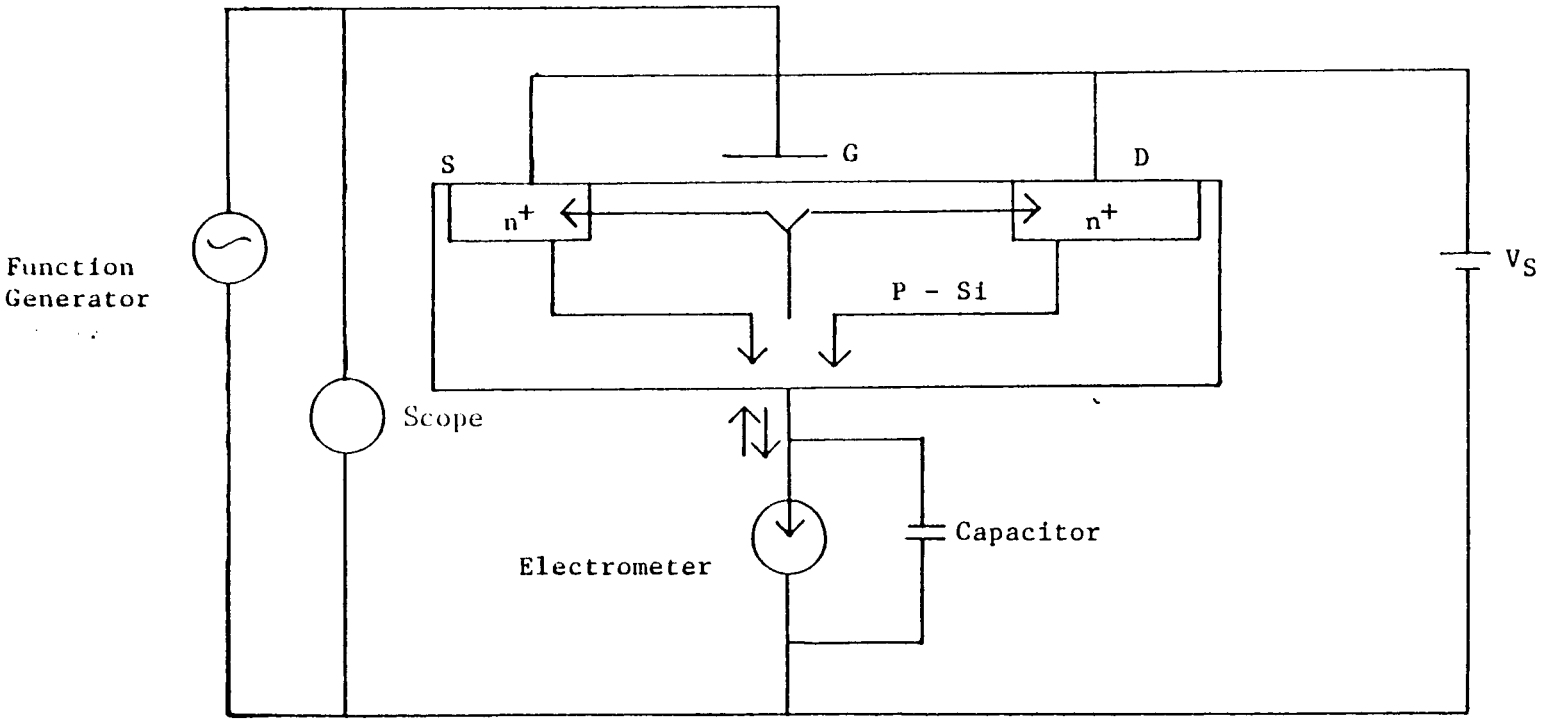


Figure 3.1 Basic Charge Pumping Experimental Set-Up

into inversion, the surface becomes deeply depleted and electrons will flow from the source and drain region into the channel, where some of them will be captured by the surface states. When the gate pulse is driving the surface back into accumulation, the mobile charge drifts back to the source and drain under the influence of the reverse bias, but the charges trapped in the surface states will recombine with the majority carriers from the substrate, and will result in a net flow of negative charge into the substrate. This is what is called the charge pumping effect. The surface charge Qss which will recombine with the majority carriers is given by:

$$Qss = A \times q^2 \; Dit(E)\, dE \qquad (3.1)$$

It can also be expressed as:

$$Qss = A \times q^2 \; Dit \times Qs \qquad (3.2)$$

where:

A is the area of the transistor (Cm^2)

Dit(E) is the surface state density at energy level E ($cm^{-2}\ eV^{-1}$)

Dit is the mean surface-state density, averaged over the energy levels swept through by the Fermi level ($Cm^{-2}\ eV^{-1}$)

Qs is the total sweep of the surface potential and

q is the electron charge.

The Qss has been shown by the C-V measurement technique to consist of oxide fixed charge Q_f, interface trap charge Q_{it} and oxide trap charge Q_{ot}. In this case it is given by:

$$Qss = Q_f + Q_{it} + Q_{ot} \qquad (3.3)$$

When applying repetitive pulses to the gate with frequency f, this charge Qss will result in a pumped current from the source and drain to the substrate. The magnitude of the pumped current due to the surface charge Qss is given by:

$$I_{cp} = f.\ Qss$$
$$= f\ A\ q^2\ Dit\ Qs \qquad (3.4)$$

By measuring this substrate current (charge pumping current), an estimate of the mean value of the interface states density over the energy range swept by the gate pulser can be obtained.

3.1.2 MEASUREMENT OF THE CHARGE PUMPING CURRENT

The charge pumping current is measured by keeping the rise time t_r of the gate signal constant while changing the fall time t_f, or vice versa. The device should be varied to switch from strong inversion to a strong accummulation.

To achieve this, the device's threshold voltage V_{TH} must be measured, and its flatband voltage V_{FB} estimated as well as a convenient selection of the peak and base levels - V_{gp} and V_{gb}, respectively, of gate wave form. To ensure strong inversion,

$$V_{gp} - V_{TH} > Vs \qquad (3.5)$$

and to ensure strong accumulation

$$V_{gb} < V_{FB} \qquad (3.6)$$

When the transistor is cycled between the accumulation

and inversion regions, three different modes, each corresponding to the conventional operating regions of the MOS structure (accumulation, depletion and inversion), are encountered.

Considering a p-type substrate (n-channel device) as used in this work, a waveform as shown in Fig. 3.2 is applied to the transistor gate. $V_g = V_{gp} - V_{gb}$ is the amplitude, and Tp is the period. When the surface is in accumulation (V_g negative), all of the surface states below the quasi-Fermi level of the minority carriers are filled with electrons, while those above it are empty. The states are thus in equilibrium with the energy band. When the surface is in depletion ($V_g > 0$), the concentration of free carriers (holes and electrons) is very small and the majority carriers (holes) of the substrate cannot recombine with the trapped carriers in the surface state because of the potential barrier between the substrate and the surface. When the surface is in inversion, and the gate voltage is close to the threshold voltage V_{TH}, electrons will be trapped in the surface state not yet emptied (of holes). This process will become more significant when $V_g = V_{TH}$. When $V_g > V_{TH}$ (strong inversion), the remaining traps will be filled by electrons coming to the source and the drain junction.

When the gate is pulsed back, similar mechanisms are in operation. First, electrons are emitted from the surface states and flow back to source and drain until approximately the threshold voltage is reached. Then, in the depletion region, emission of electrons from the surface states to the conduction band will occur, followed by removal through source and drain. Finally, when the gate voltage is approximately equal to the flat

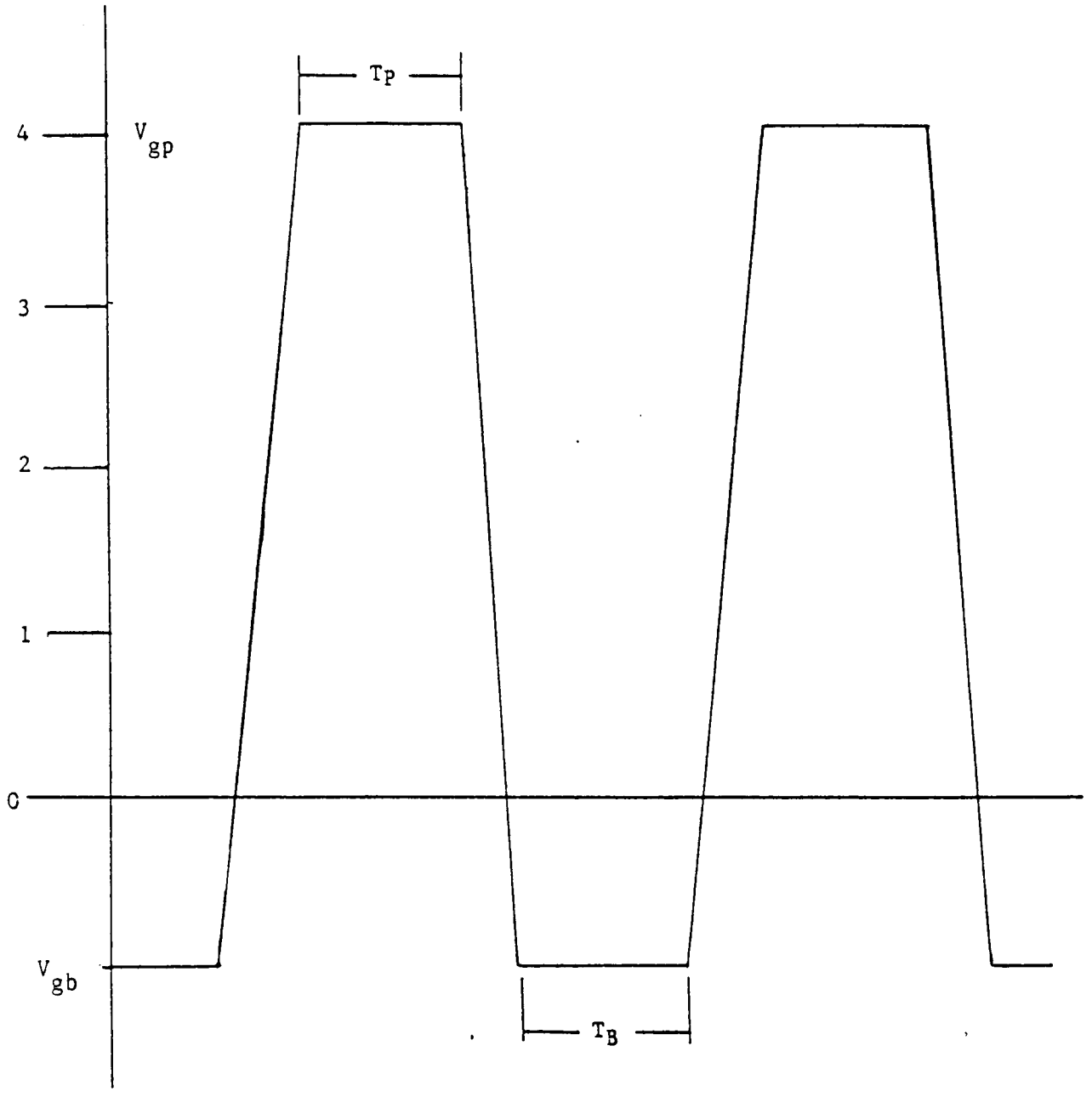


Figure 3.2 Waveform Used for Charge Pumping Experiments

band voltage, V_{FB}, holes will fill the remaining occupied traps (with electrons). Then the substrate current measured across the electrometer is the charge pumping current given by Equation (3.4).

3.1.3 DETERMINATION OF INTERFACE STATE DISTRIBUTION

Cilingiroglu [22] and Groeseneken et al [23] have shown that when applying square pulses with variable fall times while keeping the rise time constant, one scans the energy range in the upper half of the band gap between the conduction band and the midgap. On the other hand, when varying the rise time while keeping the fall time constant, the energy states in the lower half of the band gap are scanned. The charge Qss that recombines during every cycle is given as:

$$Qss = q\ A \int_{E1}^{E2} Dit(E)\ dE \qquad (3.7)$$

where:

E1 and E2 are the boundaries of energy range (valence and conduction band, respectively).

The derivative of Qss with respect to rise and fall times of the pulse is given:

$$dQss/dti = q\ A\ [Dit(E2)\ dE2/dt1 - Dit(E1)\ dE1/dt1] \qquad (3.8)$$

E2 and E1 depend on fall and rise times, respectively. But,

$$Qss = I_{cp}/f$$

therefore the derivative becomes:

$$dI_{cp}/dt1 = f\ q\ A\ [Dit(E2)\ dE2/dt1 - Dit(E1)\ dE1/dt1] \quad (3.9)$$

Since E1 is independent of fall time, keeping rise time constant

$$dI_{cp}/dt_f = f\ q\ A\ Dit(E2)\ dE2/dt_f \quad (3.10)$$

Normalizing the energy to KT/q

$$dE2 = -\ KT/t_f \quad (3.11)$$

Therefore:

$$Dit(E2) = t_f/[q\ A\ K\ T\ f]\ x\ dI_{cp}/dt_f \quad (3.12)$$

By keeping the fall time constant and changing the rise time

$$Dit(E1) = -t_r/[q\ A\ K\ T\ f]\ x\ dI_{cp}/dt_r \quad (3.13)$$

Therefore, by measuring the charge pumping current with variable rise and fall times, one can easily obtain the interface state density as well as its energy distribution in a large part of the forbidden energy gap.

3.2. EXPERIMENTAL CONDITIONS

The two n-channel (p-type substrate) test MOS devices Q-6 and Q-28 used in this experiment were prepared by AT&T Bell Laboratories, Allentown, Pennsylvania. Table 3.1 shows the dimensions of the test devices. Initial and final electrical characterizations of the devices and the interface states density determination before and after proton radiation were performed in the Thomas N. Fogarty Solid State Laboratory, Prairie View A&M University. The Lehigh University Sherman Fairchild laboratory Van de Graaff accelerator was used to generate a beam of high energy proton of kinetic energy 1 MeV.

To ensure that only the silicon material of the device

TABLE 3.1 DIMESNSIONS OF TEST DEVICES

DEVICE	Q-6		Q-28	
	3.5	5.0	3.5	5.0
Channel length (micron)	3.5	5.0	3.5	5.0
Ioff (mA)	10.02	10.03	10.02	10.03
Ion (mA)	5.76	4.69	6.12	4.73
Beta	980.40	817.30	1113.9	826.10
Channel width (micron)	50	50	50	50
V_{TH} (Volts)	0.82	0.81	0.80	0.80

was exposed to proton radiation, the encapsulation of device Q-6 was removed, followed by the removal of an alpha-particle resistant silicone rubber (RTV) deposited on the device during manufacturing process, using trimethyl guanadine transistor Q-28 was irradiated with encapsulation on. This demonstrated that device radiation damage for the same dose rate was dependent on structure of the resistant layer. Even though proton radiation was stopped, secondary radiation caused similar parameter shifts.

Each of the two devices has two transistors of 3.5 micron and 5.0 micron. It is pertinent to mention that the 3.5 micron transistors were kept under +4.5 V bias during and after irradiation. Whereas the 5.0 micron transistors were kept on zero bias. A photomicrograph of Q-6 is shown in figure 3.3.

Both devices were subjected to 0.822 X 10^6 Rads (Si) of 1 MeV proton radiation for 60 seconds at 27^o C. After irradiation the devices were left in chamber at room temperature between measurements. Changes in transconductance, threshold voltage and charge pumping current variations after irradiation have been used as a measure of degradation and rebound effects. The transconductance Gm was measured at constant drain voltage Vd =1 V to 5 V at five levels. The threshold voltage is defined as an extrapolation of the linear I-V characteristics at Vg intercept. The charge pumping measurements were performed using pulses with a frequency of 100 Hz, a constant amplitude V_{gp} = 4 V, and V_{gb} = - 1 V. The charge pumping variations with frequency, reverse bias voltage (V_{rev}) and gate voltage pulses were performed using a computer program written by Kalu Diogu [24].

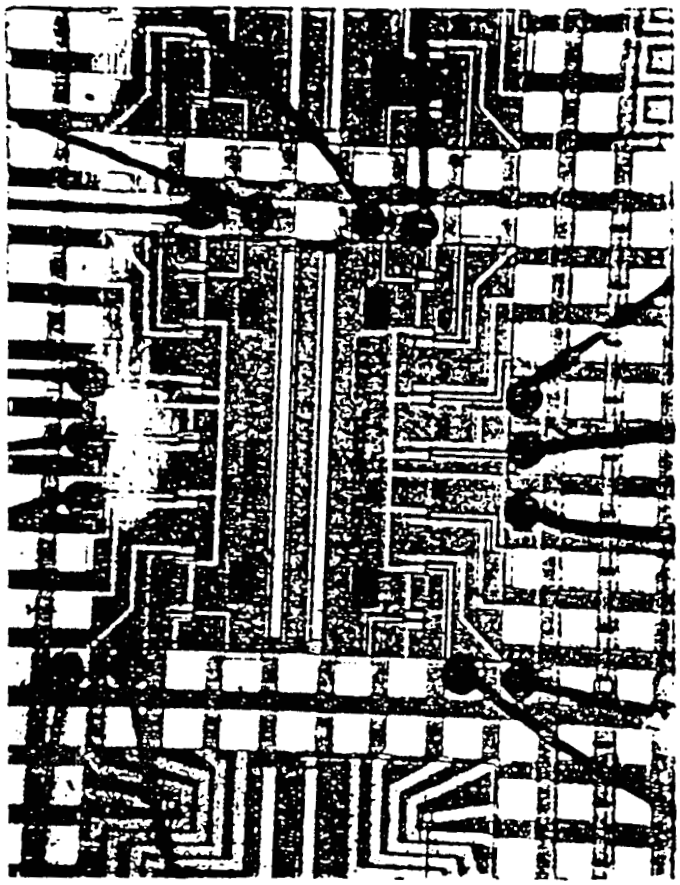


Figure 3.3 Photomicrograph of the NMOS Device

C-2

3.3 RESULTS AND DISCUSSIONS

Figure 3.4 shows the transconductance (Gm) as a function of gate voltage (Vg) for a fixed drain voltage Vd = 2.0V, source voltage Vs = 0V, and substrate voltage Vsub = 0V, before and after 1000 hrs post radiation anneal for device Q-28. Figure 3.5 shows the same relationship for device Q-6.

In both cases, the negative shifts in transconductance after irradiation, which is a measure of transconductance degradation, is due to hole trapping. At the top regions of the Gm versus Vg curves, a steep decrease in transconductance after radiation which has been reported for small gate area transistors, is observed. However, we have not been able to account for it.

Figure 3.6 shows I-V characteristics for threshold voltage (V_{TH}) determined before and after irradiation for device Q-28. Figure 3.7 shows the same relationship for device Q-6. A sharp decrease in current accompanied by a slope degradation in the subthreshold region is observed after irradiation. The decrease in current is attributed to the build-up of negative charges from acceptor-like interface states in the upper half of the silicon band gap, while the subthreshold slope change is due to an increase in interface states density (Dit) which is a measure of the threshold voltage shift after irradiation as indicated in the curve of figure 3.7 We believe that the decrease in current is due partially to boron redistribution on the glassy oxide side of the interface since the activation energy comes from the proton radiation.

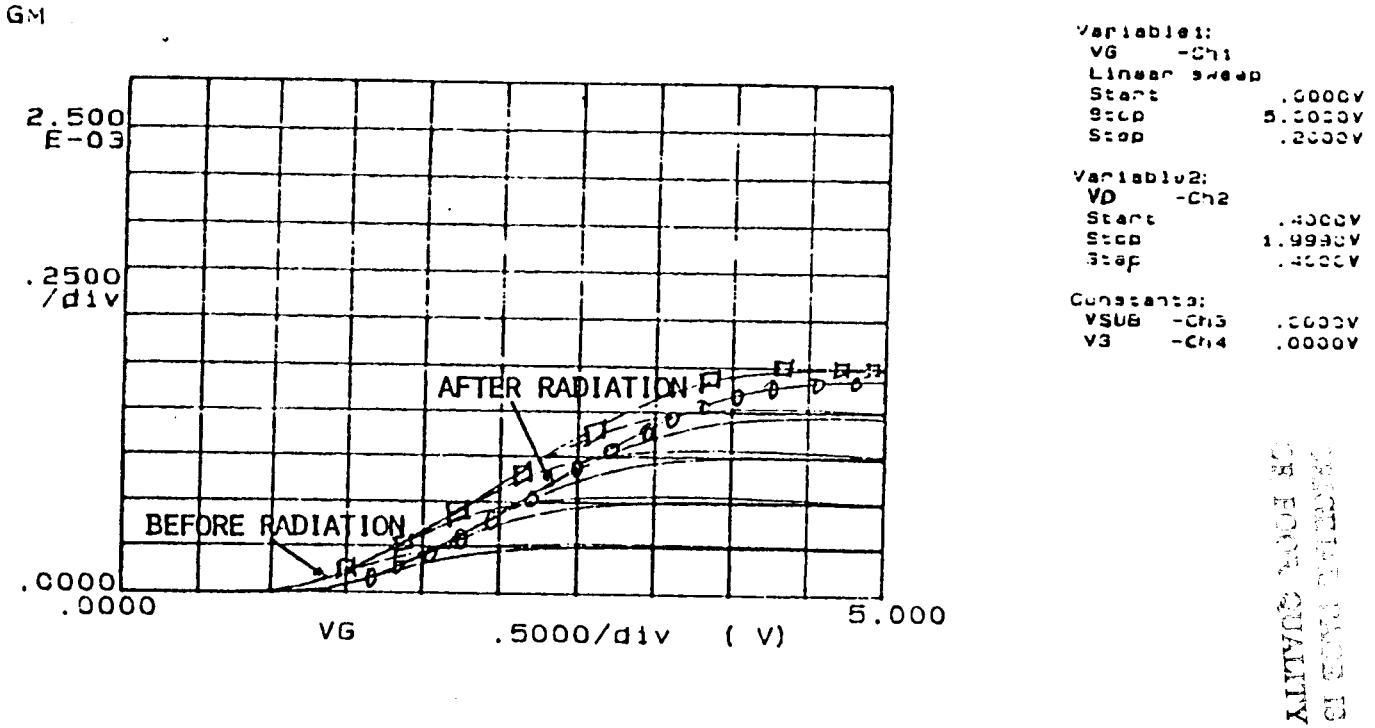


Figure 3.4 Transconductance versus Gate Voltage before and after Radiation for Q-28 (encapsulation on - secondary radiation)

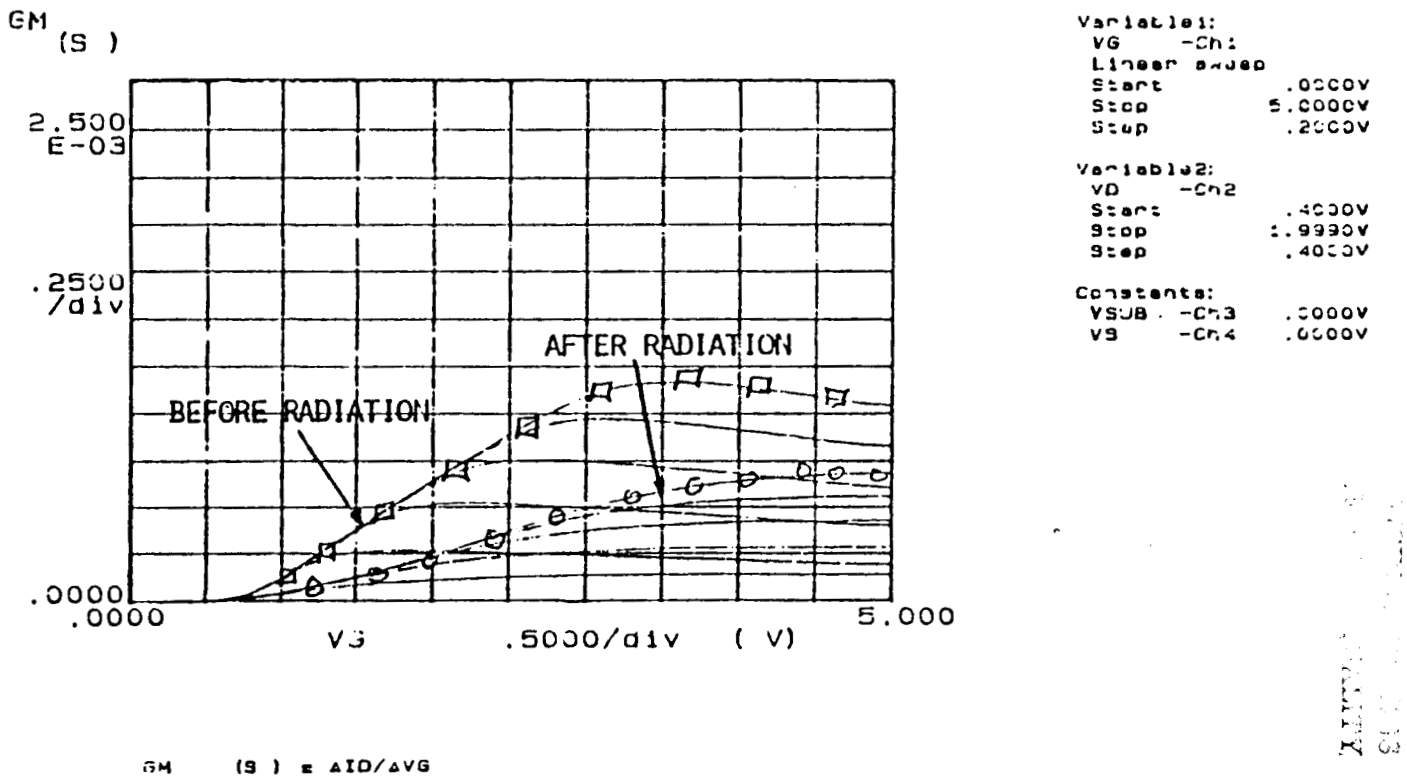
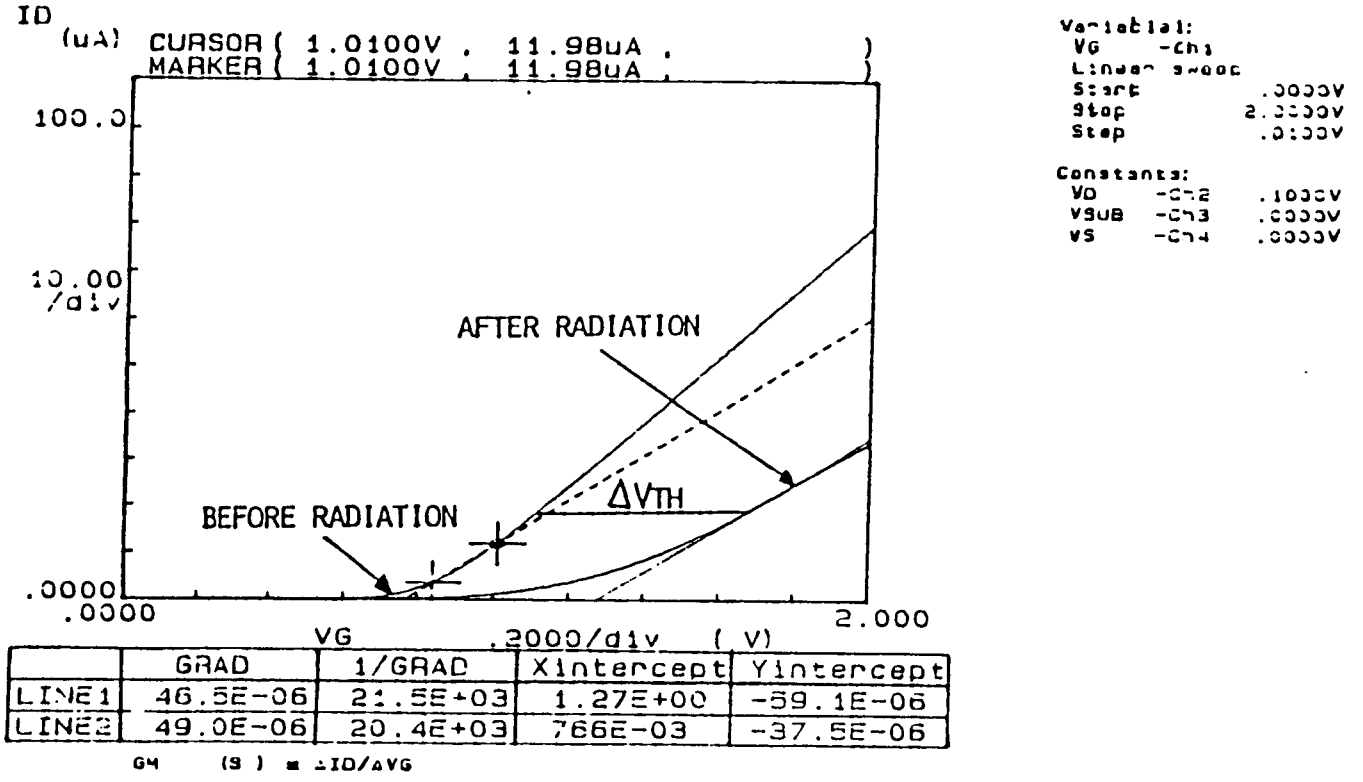


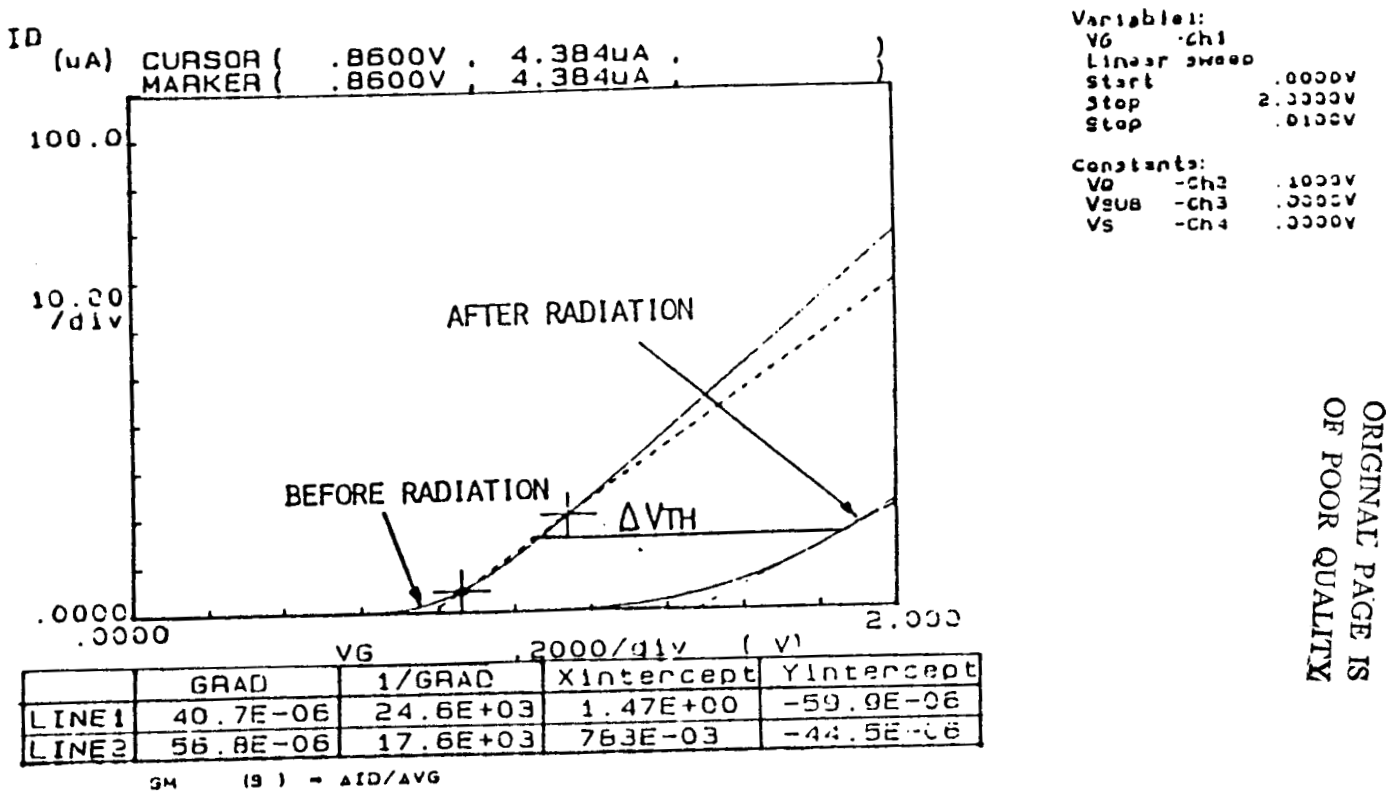
Figure 3.5 Transconductance versus Gate Voltage before and after Radiation for Q-6 (encapsulation off - proton damage)



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	46.5E-06	21.5E+03	1.27E+00	-59.1E-06
LINE2	49.0E-06	20.4E+03	766E-03	-37.5E-06

GM (S) = ΔID/ΔVG

Figure 3.6 Threshold Voltage Shifts Due to Proton Radiation for Q-28



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	40.7E-06	24.6E+03	1.47E+00	-59.9E-06
LINE2	56.8E-06	17.6E+03	763E-03	-44.5E-06

Figure 3.7 Threshold Voltage Shift Due to Proton Radiation for Q-6

In all cases, a more severe degradation in transconductance as well as threshold voltage is observed in Q-6 than in Q-28. As a result, the effect in Q-6 is attributed to proton damage, whereas in Q-28, the effect is due to secondary radiation.

Tables 3.2 and 3.3 show the experimental data for device Q-6 and Q-28, respectively. It is a tabulation of different threshold voltage changes at times during radiation and for 1000 hrs post radiation anneal. A plot of V_{TH} (volts) against time is shown in Figure 3.8 and 3.9 (for Q-6 and Q-28, respectively). On removing irradiated samples from the Van de Graaff generator there is a time lag until first measurment may be taken. Due ro rapid annealing because of hole transport effects, the negative threshold voltage shift exceeds a measured value by a considerable factor. Best estimates for the negative threshold voltage shift under these experimental conditions were obtained by irradiating several samples for variable time dosage period. Error bars are shown in figure 3.8 and 3.9, respectively. The threshold voltage (V_{TH}) shifts of both NMOS devices are shown for both biased and unbiased transistors during irradiation and post radiation anneal at 27^{o} C for V_{gs} = 4.5 V and V_{gs} = 0 V. The threshold voltage shows a rebound effect. Both curves reveal bias dependence on rebound, and an initial decrease in the threshold voltage during irradiation as positive charges build-up in the gate oxide, and an increase in the threshold voltage immediately after irradiation for Q-6. Q-28 shows a rebound effect 14 hours after irradiation. This we believe is due to the presence of the RTV in the surface of the device (an X-ray influence). In both cases however, the negative V_{TH} shift is

TABLE 3.2 Experimental data for device Q-6

V_{th} (3.5)	0.82	0.66	0.79	0.89	0.92	1.18	
Time (hours)	0	0.02	0.03	0.4	14	56	
V_{th} (5.0)	0.81	0.41	0.58	0.61	0.63	0.67	
V_{TH} (3.5)	1.33	1.39	1.46	1.50	1.54	1.56	1.55
Time (hours)	132	206	278	350	490	782	933
V_{th} (5.0)	0.70	0.73	0.76	0.80	0.80	0.81	0.81

TABLE 3.3 Experimental data for device Q-28

V_{th} (3.5u)	0.80	0.78	0.75	0.71	0.97	1.05	
Time (hour)	0	0.02	0.4	14	56	93	
V_{th} (5.0u)	0.80	0.72	0.64	0.46	0.56	0.62	
V_{th} (3.5)	1.08	1.10	1.18	1.20	1.30	1.38	1.39
Time (hours)	132	206	278	350	490	782	933
V_{th} (5.0)	0.68	0.70	0.75	0.77	0.79	0.79	0.80

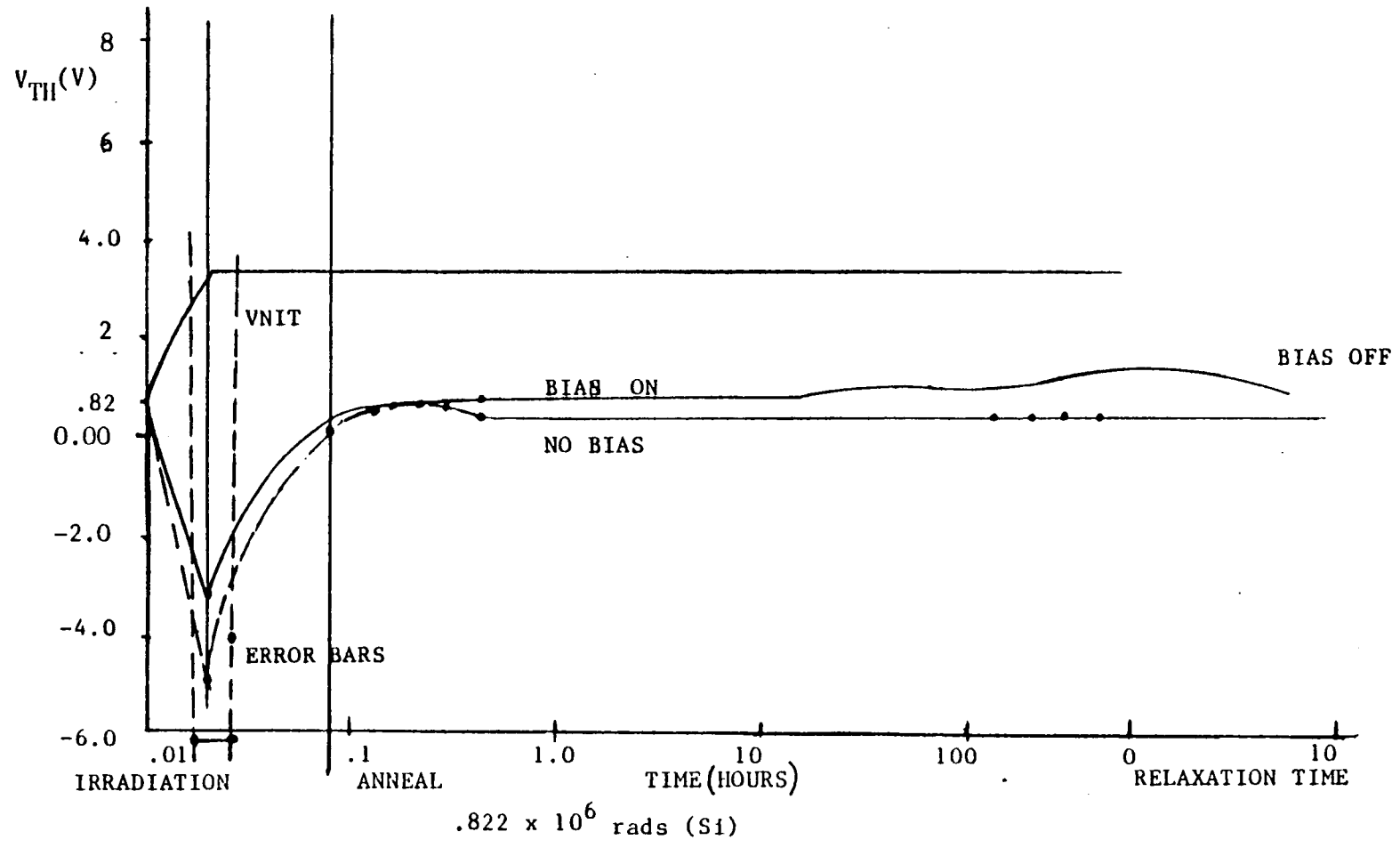


Figure 3.8 Threshold Voltage Shift of Q-6 during Radiation and Anneal (proton radiation)

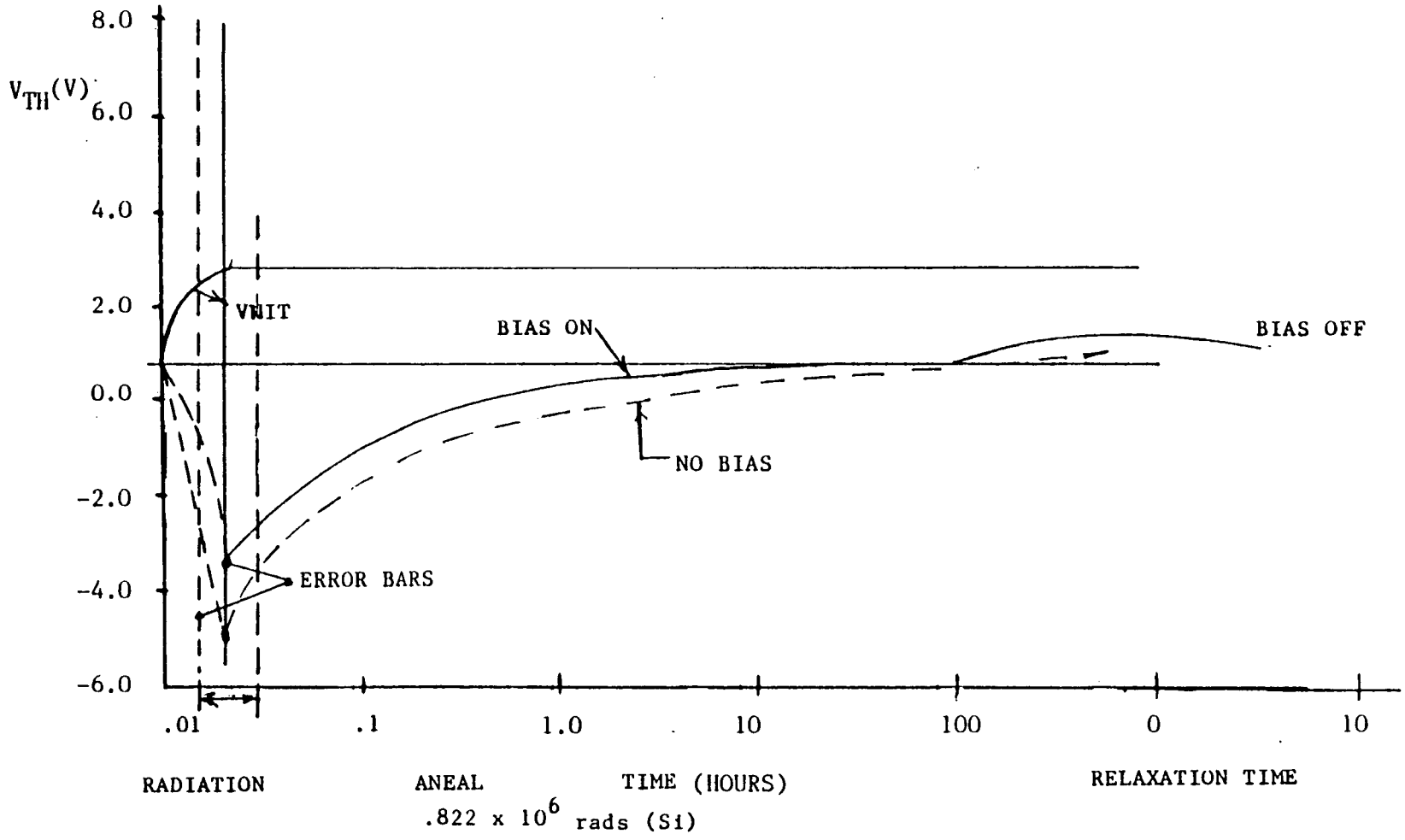


Figure 3.9 Threshold Voltage Shift of Q-28 during Radiation and Anneal (secondary radiation)

more pronounced in the unbiased transistors than in the biased transistors. For the zero biased transistors, the threshold voltage only increased back to its pre-irradiation value, whereas the 4.5V biased transistors increased to twice it pre-irradiation value. This is due to radiation induced interface states charge build-up whose contribution to the threshold voltage shifts can be calculated from:

$$Vss = Qss/C_{ox} \qquad (3.14)$$

where:

C_{ox} = oxide capacitance (F/cm^2)

Qss = surface states density = I_{cp}/f

f = frequency = 100 Hz

From Table 3.5

I_{cp} (Upper half for Q-6) = 4.3 uA

I_{cp} (Upper half for Q-28) = 3.8uA

Qss(for Q-6) = 4.3×10^{-8}

Qss(for Q-28) = 3.8×10^{-8}

$C_{ox} = C_{ox}/t_{ox}$

t_{ox} = oxide thickness = 220 A = 220×10^{-8} cm

C_{ox} = dielectric constant = 3.2 $C_{ox} = 3.2 \times 8.8 \times 10^{-14}$

$C_{ox} = 0.128 \times 10^{-6}$

V_{ss} (for Q-6) = 3.35 V

V_{ss} (for Q-28) = 2.96 V

The results of the curves agree with Schwank et al [8] rebounds phenomena, and confirm that the gate bias affects the final saturation voltage during both irradiation and anneal at 27^{o} C. It is in agreement with the King and Martins' [3]

TABLE 3.4 Charge pumping measurements before radiation

DEVICE	f (Hz)	T_p (us)	I_{cp} (uA)	V_{gb} (V)	V_{gp} (V)	V_s (V)
3.5u	100	100	0.26	-0.4	4.0	1.0
	100	280	0.29	-0.4	4.0	1.0
	100	-280	0.23	-0.4	4.0	1.0
5.0u	100	100	.39	-0.4	4.0	1.0
	100	280	.65	-0.4	4.0	1.0
	100	-280	.16	-0.4	4.0	1.0

TABLE 3.5 Charge pumping measurements after radiation

DEVICE	f (Hz)	T_p (us)	I_{cp} (uA)	V_{gb} (V)	V_{gp} (V)	V_s (V)
3.5u	100	100	7.0	-0.4	4.0	1.0
	100	280	11.3	-0.4	4.0	1.0
	100	-280	3.2	-0.4	4.0	1.0
5.0u	100	100	0.44	-0.4	4.0	1.0
	100	280	8.4	-0.4	4.0	1.0
	100	-280	1.04	-0.4	4.0	1.0

prediction of the behavior of n-channel devices at about 10^5 rads (Si). The curves also show that during irradiation V_{Nit} increased to approximately 2.7 volts and did not change during anneal.

3.3.1 DETERMINATION OF INTERFACE STATE DENSITY

The shift caused by the interface states in the test device after irradiation can be determined by calculating the interface states distributions from the charge pump experiemtnal technique described in Section 3.1.3. These contributions are integrated over the appropriate part of the band gap to separate the Dit distribution in the upper and lower half of the silicon band gap.

The charge pumping measurements before and after 0.822×10^6 Rad (Si) of 1 MeV proton radiation results are shown in tables 3.4 and 3.5 for Q-28 and Q-6, respectively. These measurements were made as described in Section 3.1. The waveform shown in figure 3.2 was used, and the rise and fall times of the waveform were varied. The gate peak voltage V_{gb} of magnitude 4.0V is 2.2 times the difference from the threshold voltage and power supply voltage Vs. The initial current measured in strong inversion and accumulation regions was due to parasitic leakage current I_1. As the frequency was increased to 100 Hz the substrate current I_s became significant. Therefore $I_s - I_1 = I_p$.

From the tabulated results, the interface state density Dit for the device is obtained using Equation (3.12) for the upper half of the band gap, and Equation (3.13) is used for the lower half of the band gap.

For device Q-6, before radiation

Dit (3.5u) = 0.744 X 10^{10} $cm^{-2}eV^{-1}$ for upper half

Dit (3.5u) = 0.744 X 10^{10} $cm^{-2}eV^{-1}$ for lower half

Dit (5.0u) = 0.45 X 10^{10} $cm^{-2}ev^{-1}$ for upper half

Dit (5.0u) = 0.40 X 10^{10} $cm^{-2}eV^{-1}$ for lower half

For device Q-6, after radiation

Dit (3.5u) = 1.066 X 10^{11} $cm^{-2}eV^{-1}$ for upper half

Dit (3.5u) = 0.97 X 10^{11} $cm^{-2}eV^{-1}$ for lower half

Dit (5.0u) = 0.87 X 10^{11} $cm^{-2}eV^{-1}$ for upper half

Dit (5.0u) = 0.69 X 10^{11} $cm^{-2}eV^{-1}$ for lower half

The results show that for the biased transistor for Q-6 no change in charge pumping current was observed at different rise and fall times, indicating that the upper half of the band gap is completely filled with acceptor traps.

3.3.2 CHARGE PUMPING CURRENT VARIATIONS

The charge pumping technique also provides direct information on the total and the nature of interface states created after irradiation. The charge pumping current variation measurements were made immediately after irradiation. The curves of charge pumping current versus frequency before and after irradiation are shown in figure 3.10 (a) and (b) respectively. The current versus frequency was measured for V_{gp} = 5V, V_{gb} = -5V, and V_s = V_d = 0V. In both cases, charge pumping current I_{cp} increases with increase in frequency. The increase in charge pumping current DI_{cp} for the same frequency after irradiation is

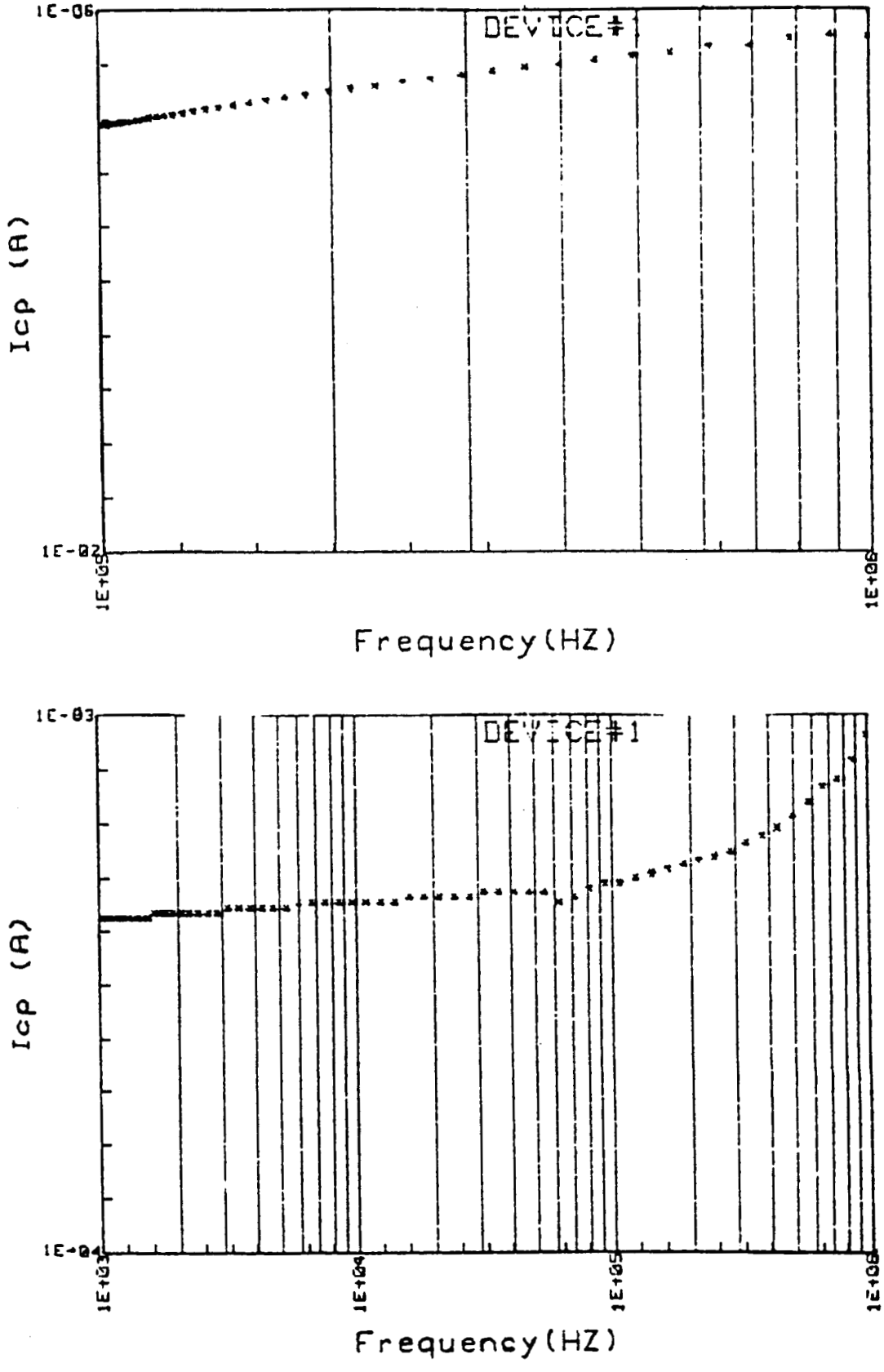


Figure 3.10 Charge Pumping Current versus Frequency (a)before and (b) after Radiation

due to the increase in interface states density (Dit).

Figure 3.11 (a) and (b) shows the charge pumping current against reverse bias voltage (Vrev). It is observed that the damage created by the proton radiation caused a significant increase in I_{cp} as well as a shift along the voltage axis, indicating a large number of fast states created during irradiation. This is evident form the decrease in I_{cp} observed in the depletion region due to channel shortening effects. Distortions are alse observed at the edges of the I_{cp} versus Vrev curve after irradiation. The rising and falling edges indicate that the net traps are of acceptor type.

The charge pumping current I_{cp} is recorded as a function of the pulsed gate voltage Vg. As shown in figure 3.12 (a) and (b) before and after irradiation, it is observed that as the Vg pulse is increased, the surface states contribution to the charge pumping current increases very strongly because of a slow change in the surface potential in the accumulation region. As the Vg pulses goes more positive, the surface states can no longer be filled by holes from source and drain regions resulting in a sharp decrease in I_{cp}. It is seen that after irradiation the peak I_{cp} value increases to a very large value due to interface states contributions. The rising edge corresponds to threshold voltage shifts and the amplitude corresponds to the number of interface states which can be determined by varying the rise and fall times of the generated waveform at constant frequency. It is pertinent to mention that all the variations in the measurements were made at 100 KHz, and that a large increase in charge pumping current is observed in all cases revealing a large

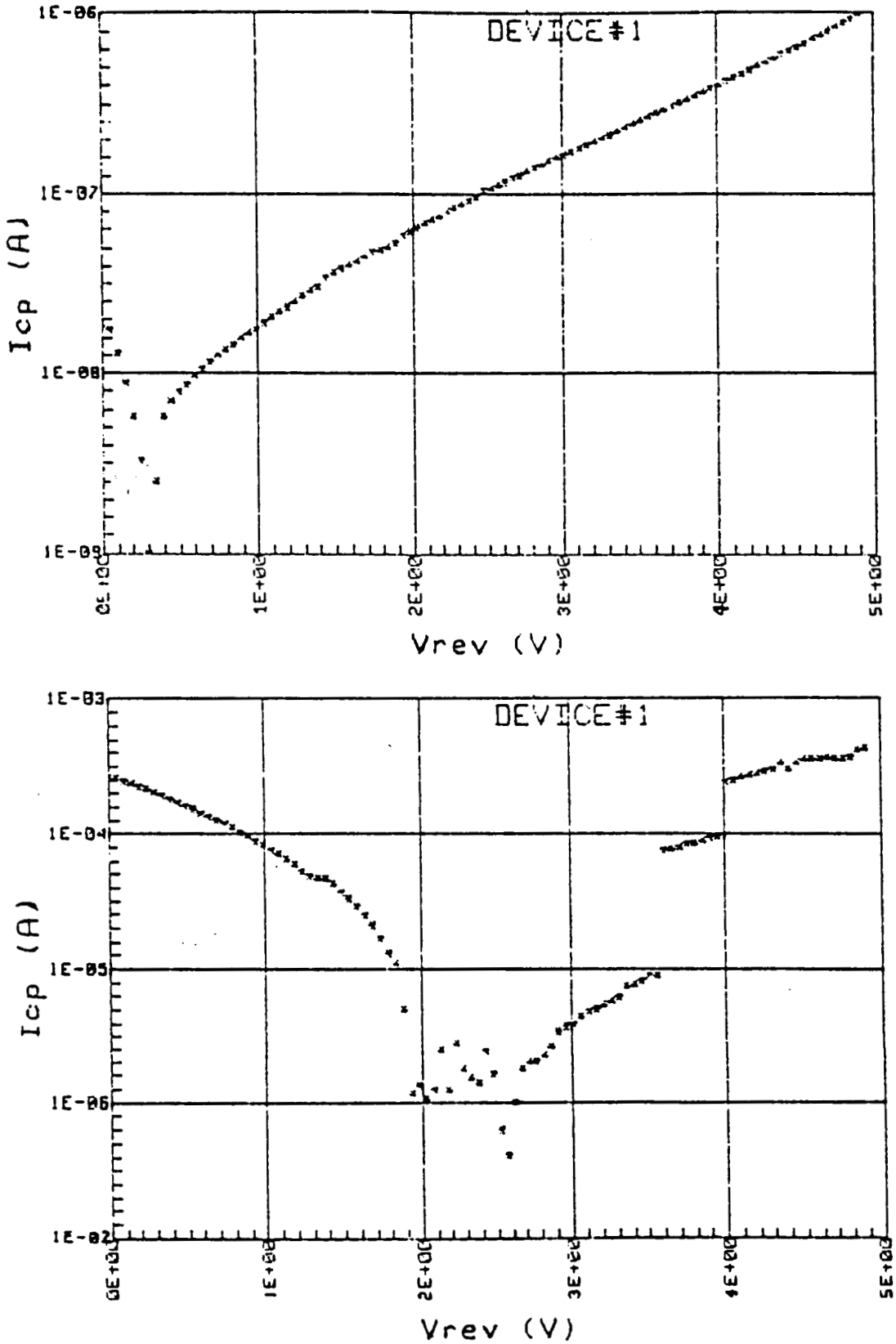


Figure 3.11 Charge Pumping Current versus Reverse Bias Voltage (Vrev) (a) before and (b) after Radiation

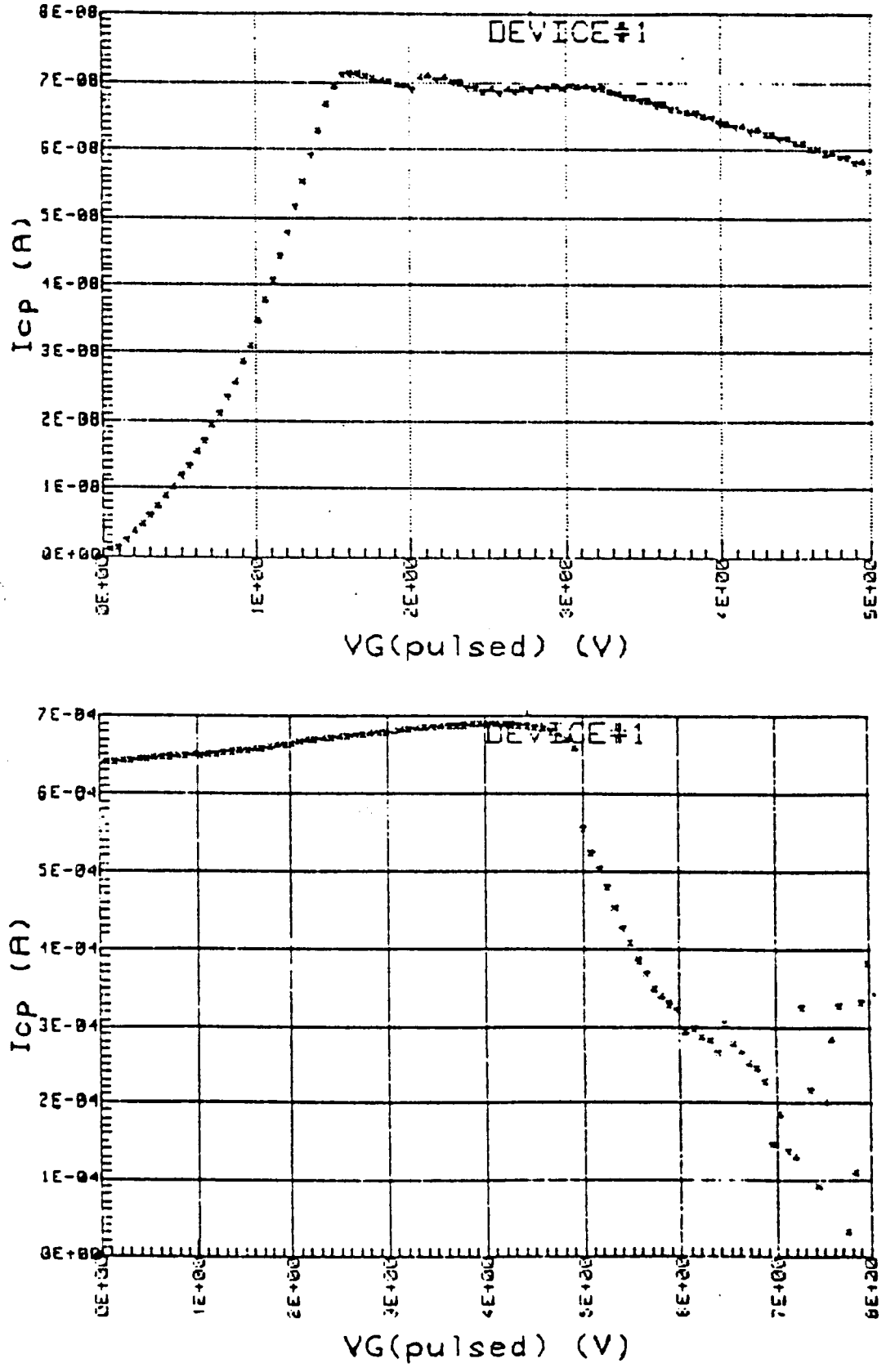


Figure 3.12 Charge Pumping Current versus Pulsed Gate Voltage (a) before and (b) after Radiation

number of fast states created during irradiation.

CHAPTER IV

HARDENING CMOS SRAM AGAINST SEU

4.1 SINGLE EVENT UPSETS IN MEMORIES

Spaceborne electronic systems employ memory elements for computing and storage. A change of logic state due to radiation can lead to, among other things, a change in data word, incorrect data transmission or reception, arithmetic data incorrectly computed, incorrect operation of software due to incorrect branching. Upsets of the above type can take place when a charged particle, such as cosmic ray or an alpha particle, strikes a sensitive part of a memory cell and sufficient charge is generated to cause a change in the logic state of the cell. From the device level, the carriers generated when a charged particle strikes a pn junction distorts the electric field in such a way that carriers tend to be collected rapidly by drift rather than by the slow process of diffusion [25]. The enhanced charge collection through fast and high amplitude drift currents makes circuits more sensitive to single event upset than if the charge collection was through slow and low amplitude diffusion currents.

In the case of CMOS static random access memory (SRAM), a charge particle striking the drain diffusion of either the p-channel or n-channel device can cause cell upset if enough charge is deposited or removed at specific nodes of the cell [26]. Two main techniques that are used to harden CMOS SRAMs against single event upsets are the use of feedback resistors and capacitors

[26,27]. These elements tend to increase the time constants of the feedback paths between the inverter pairs of the SRAM cell. The net effect is an increase in the critical charge needed cause cell upset.

Although, it has been mentioned by some investigators [28,29] that transistor sizing affects the critical charge needed to cause cell upset, no definite study has been reported in the literature showing the effect of transistor sizing on single event hardening of CMOS SRAMs. This chapter presents results on the effect of transistor sizing on hardening CMOS SRAMs against single event upsets.

4.2 METHOD

Figure 4.1 shows the circuit diagram of a CMOS SRAM cell. The cell is a flip-flop formed from two cross-coupled CMOS inverters. A single, high energy particle can strike the drain of either the p-channel or n-channel device. The charged particle, penetrating the device, will produce a number of carriers determined by its initial energy. The generated carriers, collected within the depletion regions, appear as augmented leakage current or "photocurrent" within the affected device. Figure 4.2 shows the current sources used to model the perturbing currents. "NHIT" and "PHIT" are currents used to represent ions hitting the off n- channel and p-channel transistors, respectively [26]. Cell upsets will take place if enough charge is delivered to the "hit" node. The charge is determined as an integral of the current pulse over time, and is designated as the critical charge required for upset, Q_{crit}.

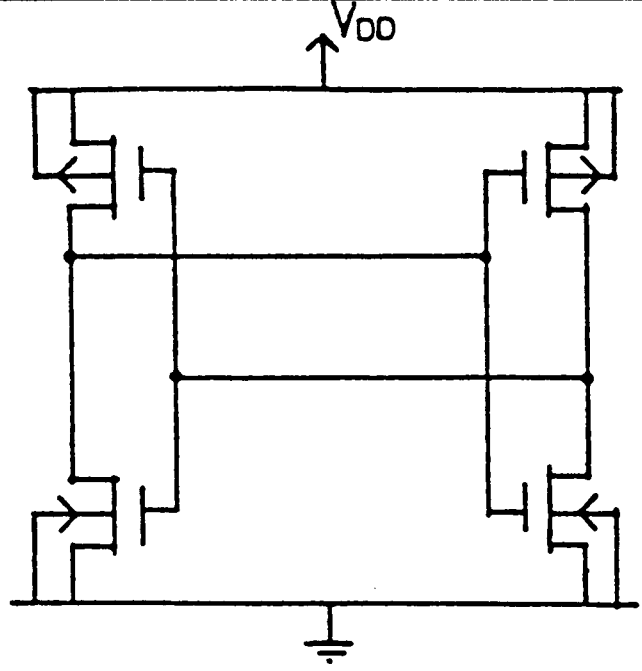


Figure 4.1 CMOS Static RAM cell

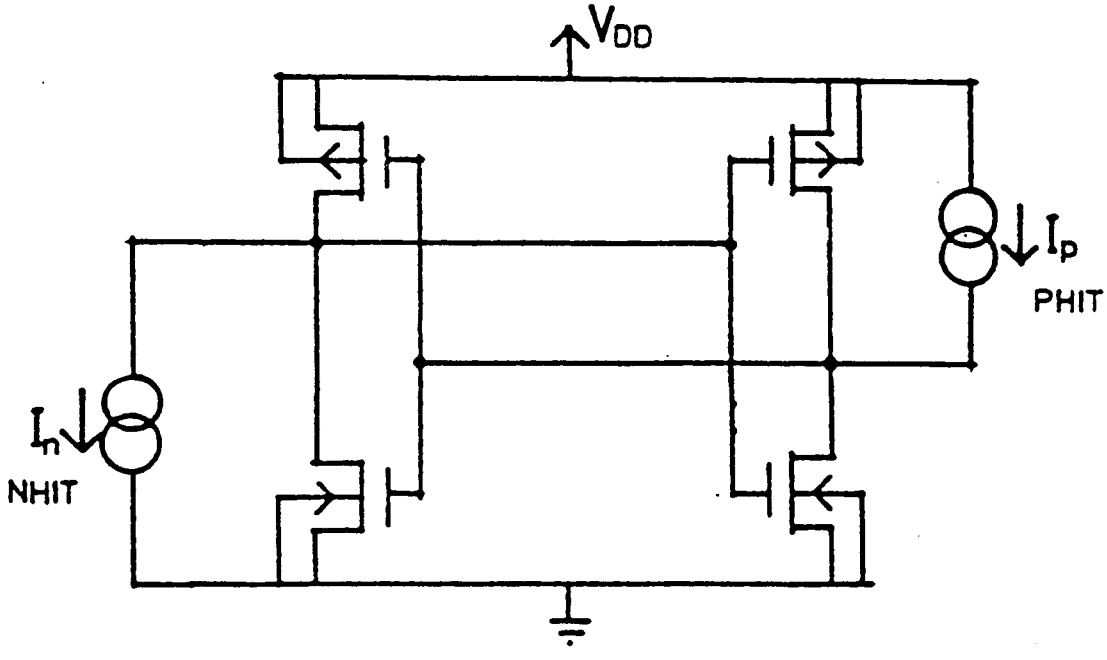


Figure 4.2 CMOS SRAM Cell with current source model for particle hit

Two methods were considered for determining the effect of transistor sizing on the hardening of CMOS SRAM. The first involves the calculation of critical charge needed to cause cell upset, the second, the determination of noise margins for the cells.

a) Calculation of Critical Charge

The critical charge is calculated using the expression:

$$Q_{crit} = \int_0^{\infty} i(t)dt \qquad (4.1)$$

where:

i(t) is a exponential decay current with time constant of 250ps [26].

i(t) is used to represent ions hitting the off n-channel or p-channel transistor. In the simulation study, the amplitude of i(t) is varied and the network analysis package, SPICE [30], was used to determine what current amplitude will cause the cell upset. Equation (4.1) can then be used to calculate the critical charge.

b) Noise Margin Calculation

Single event phenomena in digital circuits can be modeled as noise voltage superimposed on static logic levels that the circuit can tolerate before changing state. A parameter that permits one to determine the allowable noise voltage on the input of a gate so that the output will not be affected is noise margin.

Noise margin is specified by two parameters: Low noise

margin (NML) and High noise margin (NMH). The LOW and HIGH noise margins are defined by the following expressions [31]:

$$NML = |V_{IL} - V_{OL}|$$
$$NMH = |V_{OH} - V_{IH}| \qquad (4.2)$$

where:

V_{IH} is minimum HIGH input voltage

V_{IL} is maximum LOW input voltage

V_{OH} is minimum HIGH output voltage

V_{OL} is maximum LOW output voltage

As shown in Figure 4.3, V_{IH}, V_{IL}, V_{OH} and V_{OL} are obtained from the transfer characteristics. In this work, the noise margins of various CMOS circuits were determined and their dependence of the transistor sizing were obtained. Results reported in this paper are based on the use of noise margin calculations to evaluate the effect of transistor sizing on hardening CMOS SRAM.

4.3 RESULTS AND DISCUSSION

As mentioned earlier, CMOS SRAM cell is a flip-flop formed from two cross-coupled CMOS inverters. Since it is known that transistor sizing affects the switching characteristics of CMOS inverters [31], and CMOS SRAM cell is a flip-flop formed from two cross-coupled CMOS Inverters, it is imaginable to think, that the switching characteristics of CMOS SRAM might be dependent on transistor sizing. Figure 4.4 shown the transfer characteristic of CMOS SRAM. The transistor sizing is described by geometrical beta ratio defined by B_r:

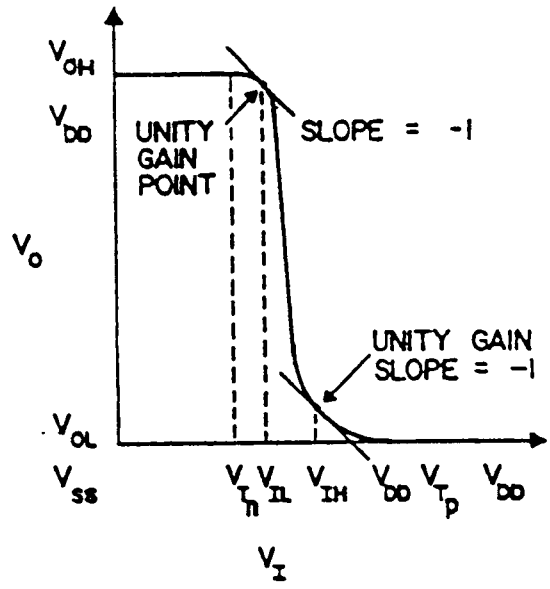


Figure 4.3 Transfer characteristic curve for determining the noise margins
(From Weste and Eshraghian [31])

$$B_r = B_n / B_p$$
$$B_n = W_n / L_n$$
$$B_p = W_p / L_p \qquad (4.3)$$

where:

W_n and W_p are the channel width of n- and p-device, and L_n and L_p are the channel length of the n- and p- device, respectively.

It should be noted that the switching characteristics of CMOS SRAM is dependent on the beta ratio. The transfer characteristics of CMOS SRAM with feedback resistors of 100k was also obtained. The curve is shown in Figure 4.5. From the transfer curves of the various CMOS circuits, the noise margins were determined.

Table 4.1 shows the noise margins for the various CMOS circuits. It can be seen from the Table that as the beta ratio increases, the low noise margin decreases and the high noise margin increases for all the circuits. It should also be noted that the values for the low noise margin are relatively smaller than those of the high noise margin. The effective noise margins of the circuits were determined from those of the low noise margin. It is interesting to note that for a particular beta ratio, the effective noise margin for the CMOS SRAM with feedback resistors is greater than that of the SRAM without feedback resistors. This observation agrees with the previously reported result that CMOS SRAM cells with feedback resistors are more hardened against single event upsets than CMOS SRAM cell without feedback resistors [26].

Table 4.1 Noise Margins for Various CMOS Circuits

	NML (V)			NMH (V)		
	B_R=0.5	B_R=1	B_R=2	B_R=0.5	B_R=1	B_R=2
CMOS INVERTER	3.6	2.7	2.0	4.8	5.4	6.2
SRAM WITHOUT FEEDBACK RESISTORS	3.5	2.5	1.9	4.8	5.5	6.4
SRAM WITH FEEDBACK RESISTORS	3.8	2.9	2.1	4.9	5.7	6.5

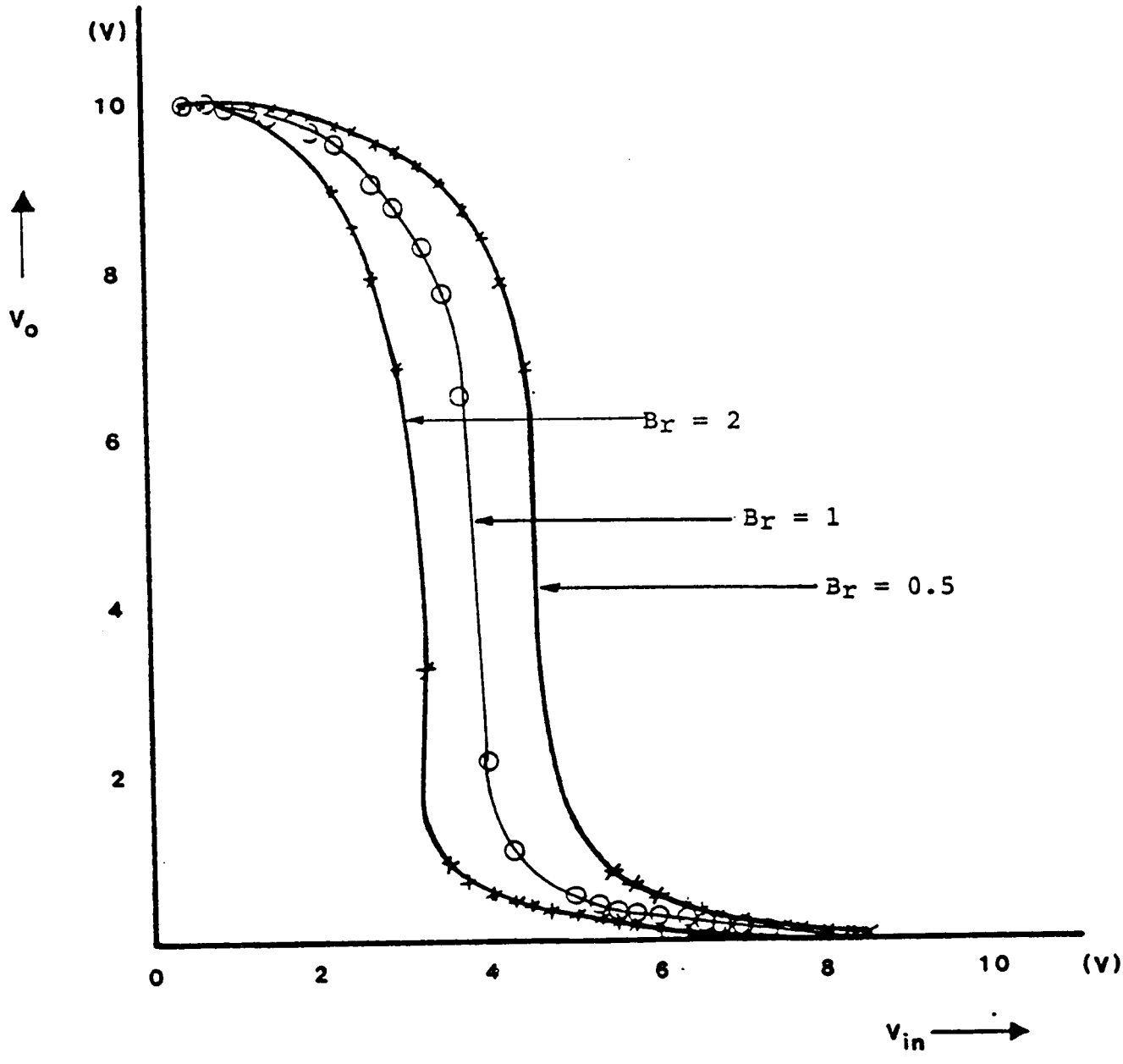


Figure 4.4 Transfer characteristics for CMOS SRAM without feedback resistors for various beta ratios

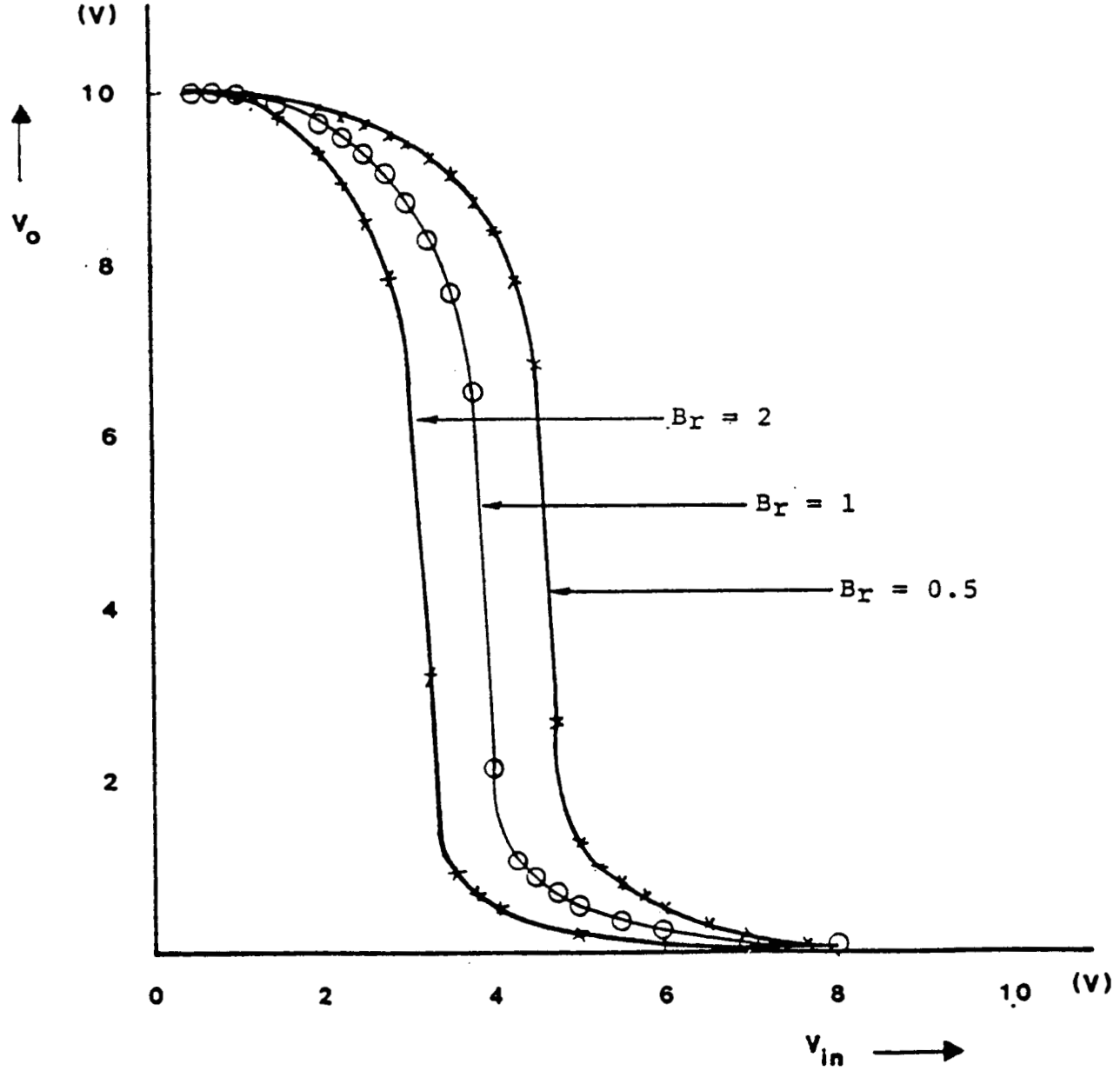


Figure 4.5 Transfer characteristics for CMOS SRAM with feedback resistors for various beta ratios

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This research could not have began without the assistance of Dr. Thomas N. Fogarty, AT&T Bell Laboratories Adjunct Professor in the College of Engineering, Prairie View A&M University. He wrote the initial proposal for this research and directed the work at its inception. In addition, he served as the technical advisor during the duration of the project, was intrumental in getting me interested in the study of radiation damage of VLSI devices and supervised two graduate students Master of Science thesis. The two students, Ms. Sharon Knotts and Mr. Kalu Diogu did significant portions of the work. I am especially endebted to Dr. Fogarty and I am very thankful for all that he did towards the completion of this work.

I would also like to thank AT&T Bell Laboratories for providing us with some of the devices for this work, for allowing us to use their facilities at Allentown, Pennsylvania for some of our experiments and extending the stay of Dr. T.N. Fogarty at Prairie View A&M University in order for this work to be completed.

Ms. Sharon Knotts did her Master's thesis work on the effects of electron radiation of VLSI devices determined from C-V measurements. Chapter two of this report is from her thesis. In-

addition, Kalu Diogu did his Master of Science thesis on the effect of Proton radiation of NMOS devices determined from the charge pumping technique. Chapter three of this report is essentially a reproduction of his thesis work. The thesis work of Kalu Diogu and Sharon Knotts were very valuable to this effort. I would also like to mention undergraduate students, so many to name them all, who worked in various small projects associated with this work. My special thanks goes to all the students.

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APPENDIX

NATURAL SPACE RADIATION AND VLSI TECHNOLOGY CONFERENCE

The Natural Space Radiation and VLSI Technology conference, jointly sponsored by Prairie View A&M University and NASA, was held on January 20 and 21, 1987 at the NASA Johnson Space Center. The conference was attended by approximately two hundred scientists, engineers and technologists. A number of academic institutions, industrial organizations and national laboratories from various parts of the world particapated in the conference.

The motivation for the conference arose out of NASA's concern over the damaged cause in integrated circuits by low energy, low-dose natural space radiation (mainly electrons, protons and alpha particles). The conference provided a forum for exchange of ideas between the device physicists and the avionics communities. Some topics discussed are device physics, failure mechanisms and design of radiation hardened circuits.

There was a total of four technical sessions and three workshops. The titles of the technical sessions, workshops and the papers presented at the conference can be found in the agenda of conference (found at the end of this paragraph). Judging from the response of the participants, the conference was a major success. Several participants inquired as to the frequency with which future conferences of a similar nature will be held by us.

Natural Space Radiation and VLSI Technology Conference
January 20 and 21, 1987
Johnson Space Center, Houston, Texas

SPONSORED BY:
Prairie View A & M University
NASA/Johnson Space Center
American Institute of Aeronautics and Astronautics
Institute of Electrical and Electronic Engineers

CONFERENCE CHAIRMEN
Dr. Aaron Cohen, Director, *NASA/JSC*, General Chairman
Dr. T. N. Fogarty, *AT&T-Bell Labs*, Visiting Professor, *PVAMU*, Technical Program Chairman
Mr. Richard Kennedy, *NASA/JSC*, Arrangements Chairman
Mr. Don Rhorer, *IBM*, Publicity Chairman
Dr. Lai-lun Lo, *Rockwell International*, Finance Chairman
Mr. Ralph Lawton, *McDonnell Douglas*, Conference Coordinator

PURPOSE: The low earth orbit natural ionizing radiation environment will have a significant impact on the design of future spacecraft systems. In particular, trends in modern VLSI processes are expected to have a significant effect on device susceptibility to single event upsets, and long term device parameter variation. It is expected that interfacial traps will play an important role in operating parameter shifts and in rebound effects. The conference will provide a forum for interchange of information between the device physics and avionics communities. The conference will also formalize the current issues and propose design solutions.

SUMMARY AGENDA

DATE	TIME	SESSION
Tue, Jan. 20	7:30/8:30 A.M.	REGISTRATION
Tue, Jan. 20	8:30/9:25 A.M.	OPENING REMARKS
Tue, Jan. 20	9:25/11:50 A.M.	SESSION I: NATURAL SPACE ENVIRONMENT
Tue, Jan. 20	1:00/3:30 P.M.	SESSION II: MATERIALS RESPONSE TO RADIATION
Tue, Jan. 20	3:30/5:20 P.M.	SESSION IIIA: DEVICE RESPONSE TO RADIATION
Tue, Jan. 20	6:30/7:15 P.M.	SESSION IIIA (Continued)
Tue, Jan. 20	7:15/9:15 P.M.	POSTER SESSION/LATE NEWSPAPERS
Wed, Jan. 21	8:00/9:30 A.M.	SESSION IIIB: DEVICE RESPONSE TO RADIATION
Wed, Jan. 21	9:35 A.M./1:00 P.M.	SESSION IV: SYSTEM ACCOMMODATION TO SPACE ENVIRONMENT
Wed, Jan. 21	2:15/3:30 P.M.	WORKSHOPS
Wed, Jan. 21	3:30/4:30 P.M.	SUMMARY PANEL
Wed, Jan. 21	4:30	CLOSING REMARKS

PROCEEDINGS

Each attendee will get one copy of the proceedings within 90 days following the conference.

PROGRAM SUMMARY

TUESDAY, JANUARY 20

REGISTRATION AND OVERVIEW

7:30 A.M.	REGISTRATION	
8:30 A.M.	Dr. Aaron Cohen, Director, *NASA/JSC*	Welcome and Opening
8:35 A.M.	Dr. Percy Pierre, President, *Prairie View A & M University*	Welcome on Behalf of PVAMU
8:45 A.M.	Dr. Wayne Perry, Dean of Engineering, *PVAMU,*	Remarks on Behalf of PVAMU
8:50 A.M.	Mr. Richard Kennedy, *NASA/JSC*	Logistics of Conference
8:55 A.M.	Dr. T. N. Fogarty, *AT&T-BL,* Visiting Professor, *PVAMU*	Overview by Technical Chairman

SESSION I: NATURAL SPACE ENVIRONMENT

9:05 A.M.	D. Stuart Nachtwey, *NASA/JSC*	Chairman's Remarks
9:10 A.M.	E. G. Stassinopoulos, *NASA/GSFC*	Low Earth Orbit Space Radiation Environment and Engineering Program Risks (Invited)
10:10 A.M.	L. W. Townsend & J. W. Wilson, *NASA/LaRC*	Galactic Heavy Ion Propagation through Spacecraft (Invited)
11:05 A.M.	J. W. Adolphsen, *NASA/GSFC;* M. K. House, *IBM*	CRUX III - Ground/Flight Correlation of SEU Modeling (Invited)

12:00 A.M. **LUNCH (at Gilruth Center)**

SESSION II: MATERIALS RESPONSE TO RADIATION

1:00 P.M.	A. Kumar, *PVAMU*	Chairman's Remarks
1:05 P.M.	F. Feigl, *Lehigh University*	Radiation and Defects in Silicon Dioxide (Invited)
1:45 P.M.	A. H. Edwards, *U. S. Army ERADCOM*	Theoretical Studies of Defects at Si-SiO2 Interface (Invited)
2:25 P.M.	L. P. Trombetta, *University of Houston,* & R. J. Zeto, *U. S. Army LABCOM*	Radiation Damage and Hole Trapping in High-Pressure MOS Oxides
2:50 P.M.	Bharat L. Bhuva, John J. Paulos, Sherra E. Diehl, Shin N. Hong, Roland W. Waltman, & J. H. Moreadith, *North Carolina State University*	Statistical Parameter Distribution in Total Dose Environments

3:15 P.M. **BREAK**

SESSION IIIA: DEVICE RESPONSE TO RADIATION

3:30 P.M.	B. Neece, *McDonnell Douglas*	Chairman's Remarks
3:35 P.M.	P. V. Dressendorfer, *Sandia Lab*	CMOS Hardening for Space Radiation Environments (Invited)
4:15 P.M.	A. G. Sabnis, *AT&T-Bell Labs*	Impact of VLSI Technology on Radiation Response and Hot Carrier Injection (Invited)
4:55 P.M.	P. S. Neelakantaswamy, *RIT Research Corp.,* & R. I. Turkman, *Rochester Inst. of Technology*	Analogous Influence of Ionizing Radiations and Electrical Overstressings: Damage Characterization Via Noise Parameters

5:20 P.M. **DINNER (at Gilruth Center)**

PROGRAM SUMMARY

TUESDAY EVENING, JANUARY 20

SESSION IIIA (Continued)

6:30	P. S. Winokur, *Sandia*	CMOS Device Response and Failure Mechanisms in Space Environments (Invited)

POSTER SESSION/LATE NEWSPAPERS*

(Complementary Wine and Cheese served)

7:15 P.M.	Turki S. M. Al-Saud & I-Dee Chang, *Stanford University*	Space Shuttle RCS Plumes Radiation & Temperature Measurement on Mission 51-G
7:15 P.M.	L. Adams, *ESA*	RADFETS Application to VLSI Systems in Space
7:15 P.M.	R. Tallon, *AFWL*	A Comparison of Dose Rate of Pulsed X-Ray, Pulsed Proton and Pulsed Electron Radiation on Bipolar Junctions
7:15 P.M.	D. J. Mead & J. Hine, *Marconi Electronics Devices*	Radiation Assessment of Silicon on Sapphire Devices
7:15 P.M.	K. K. Diogu & A. A. Kumar, *PVAMU;* T. N. Fogarty, *AT&T-BL;* C. F. Herman, *NASA/JSC*	Charge Anomaly at MOS Interfaces Submitted to Proton Radiation
7:15 P.M.	T. K. Sanderson, D. Mapper, J. H. Stephenson, & J. Farren, *Harwell Laboratory, U.K.;* L. Adams & R. Harboe-Sorenson, *ESA, Netherlands*	The Application of Cf-252 Fission Particles to SEU and Latch-up Testing in VLSI Devices
7:15 P.M.	D. K. Nichols & W. E. Price, *JPL*	Trends in Electronic Parts Susceptibility to SEU-Space Station Environment
7:15 P.M.	C. A. Philis & Y. Patin, *Commissariat a L'Energie Atomique*	

9:15 Gilruth Center closes

*** Additional presentations during this session are being planned**

PROGRAM SUMMARY

WEDNESDAY, JANUARY 21

SESSION IIIB: DEVICE RESPONSE TO RADIATION

8:00 A.M.	Ronald Jones, *Sandia Lab*	Chairman's Remarks
8:05 A.M.	G. Singh, K. F. Galloway & T. J. Russell, *NBS*	Observation of Rebound in Power MOSFETs
8:30 A.M.	Wm. A. Geideman & R. Zuleeg, *McDonnell Douglas*	Radiation Hard GaAs Circuits for Space Application
8:55 A.M.	Roe J. Maier, *AFWL* **WITHDRAWN**	Prediction of Damage from Low Level Long Exposure Radiation

9:20 A.M. **BREAK**

SESSION IV: SYSTEM ACCOMMODATION TO SPACE ENVIRONMENT

9:35 A.M.	J. Okyere,*PVAMU*	Chairman's Remarks
9:40 A.M.	S. E. Diehl, *North Carolina State Univ.*	SEU Hardening Approaches (Invited)
10:20 A.M.	G. Raines, *NASA/JSC*	Space Shuttle Orbiter Data Processing System Design Accommodations for Single Even Upsets
11:00 A.M.	A. K. Haque, J. Yates & D. Stevens, *South Bank Polytechnic, London, UK*	Upset Susceptibility of 64K and 256K DRAMS to Alpha Particle Irradiation
11.25 A.M.	T. R. Weatherford, J. R. Hauser & S. E. Diehl, *North Carolina State University*	Comparisons of Single Event Vulnerability of GaAs SRAMS
11:50 A.M.	W. A. Hanna, *McDonnell Douglas*	A Test Set for Remotely Controlled Radiation Effects on VLSIC/VHSIC
12:15 A.M.	W. D. Rabum, R. S. Singh, A. N. Petelin & D. Wilson, *Martin Marietta*	Test Chip for Radiation Effects
	J. A. Okyere, *Prairie View A & M University*	Effects of Transistor Sizing on Circuits for Single Event Upset Hardening of SRAM

1:00 P.M. **LUNCH (at Gilruth Center)**

2:15 P.M. WORKSHOPS, Co-Chairmen: F. Wang, *PVAMU*, & C. Herman, *NASA/JSC*
Workshops dedicated for formalizing the current issues will be held for each session topic. In addition, one or two specialized workshops will be organized to meet expressed concerns of the attendees. It is hoped that these workshops will highlight the most important problem areas that require additional information for design guidelines. Therefore, it is important for you to plan on participating actively in the workshops.

3:30 P.M. SUMMARY PANEL: INVITED SPEAKERS & SESSION CHAIRMEN

4:30 P.M. CLOSING REMARKS, Dr. Wayne Perry, Dean of Engineering, *PVAMU*